CM-A40i Reference User Manual

V2. 202205

Boardcon Embedded Design

www. boardcon. com

1. Introduction

1.1. About this Manual

This manual is intended to provide the user with an overview of the board and benefits, complete features specifications, and set up procedures. It contains important safety information as well.

1.2. Feedback and Update to this Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the Boardcon website (www.boardcon.com , www.armdesigner.com).

These include manuals, application notes, programming examples, and updated software and hardware. Check in periodically to see what's new!

When we are prioritizing work on these updated resources, feedback from customers is the number one influence, If you have questions, comments, or concerns about your product or project, please no hesitate to contact us at support@armdesigner.com.

1.3. Limited Warranty

Boardcon warrants this product to be free of defects in material and workmanship for a period of one year from date of buy. During this warranty period Boardcon will repair or replace the defective unit in accordance with the following process:

A copy of the original invoice must be included when returning the defective unit to Boardcon. This limited warranty does not cover damages resulting from lighting or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit. In no event shall Boardcon be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.

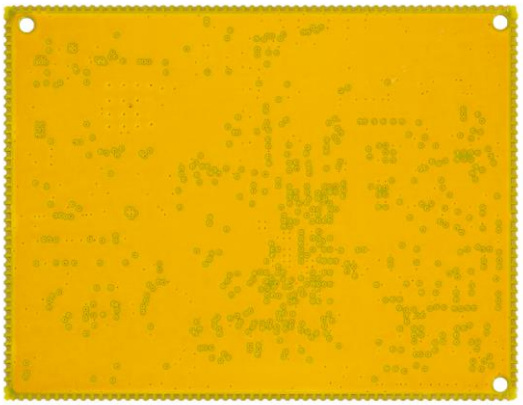
Repairs make after the expiration of the warranty period are subject to a repair charge and the cost of return shipping. Please contact Boardcon to arrange for any repair service and to obtain repair charge information.

Content

1 CM-A40i Introduction

1.1 Summary

The CM-A40i system-on-module is equipped with Allwinner's A40i quad-core Cortex-A7, Mali400 GPU, It is designed specifically for the AI devices such as industrial controller, IoT devices, intelligent interactive devices, personal computers and robots. The high performance and low power solution can help customers to introduce new technologies more quickly and enhance the overall solution efficiency.



1.2 Features

- **Microprocessor**
  - Quad-core Cortex-A7 up to 1.2G
  - 32KB I-cache,32KB D-cache,512KB L2 cache
  - Audio Codec in Core

  Memory Organization
  - DDR3L RAM up to 2GB
  - EMMC up to 32GB
- **Boot ROM**
  - Supports system code download through USB OTG
- **Security ID**
  - Size up to 2Kbit for security chip ID
- **Video Decoder/Encoder**
  - Supports video decoding up to 1080p@45fps
  - Supports H.264 encode
  - H.264 HP encoding up to 1080p@45fps
  - Picture size up t0 4096x4096
- **Display Subsystem**
  - **Video Output**

  Supports HDMI 1.4 transmitter with HDCP 1.2, up to 1080p@60fps

  Supports 4 lanes MIPI DSI up to 1080p@60fps

Supports LVDS interface up to 1920x1080@60fps

Supports RGB interface up to 1920x1080@60fps

- **Image in**

Supports TV decoder:4-ch analog CVBS or 1-ch YPbPR signal input

Supports CMOS sensor parallel interfaces

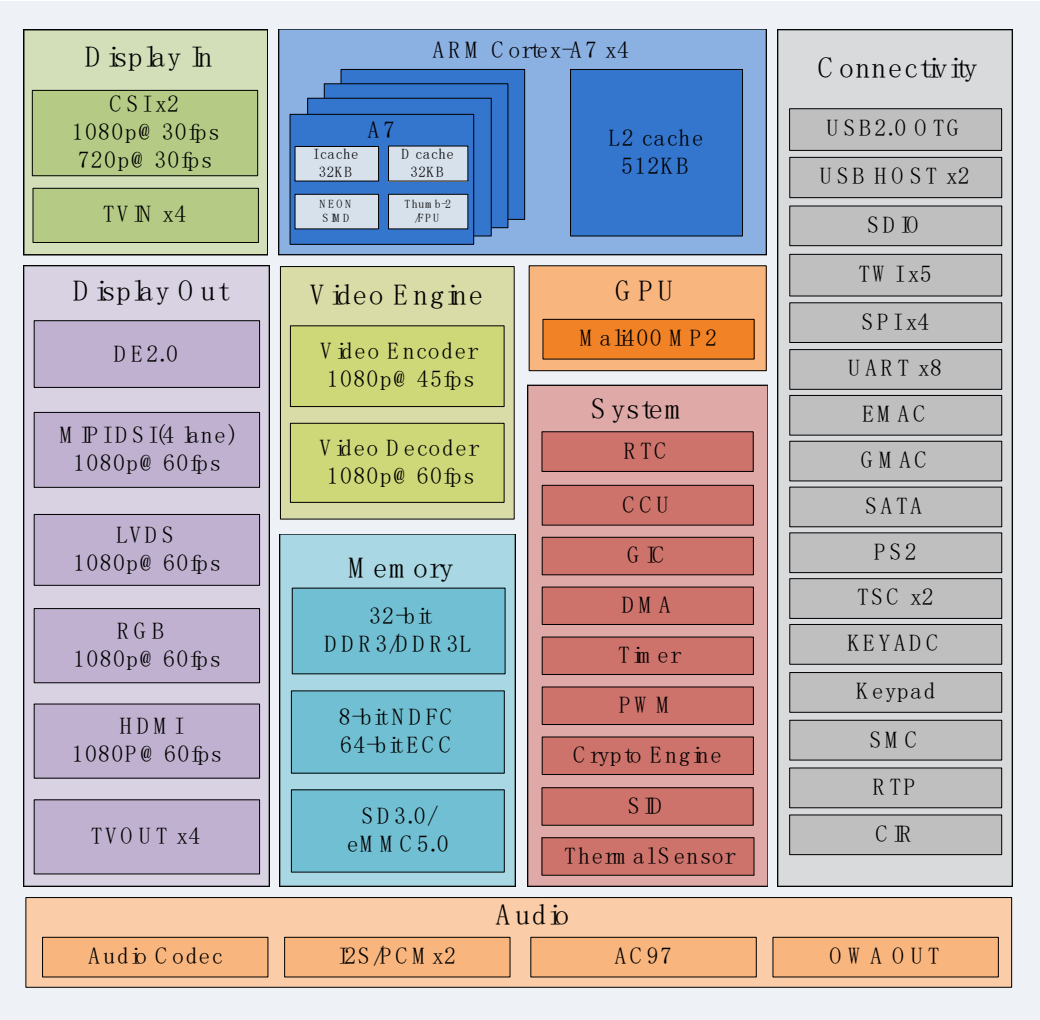
- **Analog audio inputs and outputs**
  - One mono microphone input
  - One stereo headphone output
- **I2S/PCM/ AC97**
  - One I2S/PCM interface
  - Up to 8-CH output
  - One SPDIF output
- **USB**
  - Three USB interfaces
  - One USB 2.0 OTG, and two USB hosts
- **Ethernet**
  - GMAC/EMAC
  - Support 10/100/1000Mbit/s data transfer rates
  - Support MII/RGMII PHY interface
- **I2C**
  - Up to three I2C
  - Support standard mode and fast mode(up to 400kbit/s)
- **Smart Card Reader**
  - Support ISO/IEC 7816-3 and EMV2000(4.0) specifications
  - Support synchronous and any other non-ISO 7816 and non-EMVcards
- **SPI**
  - Up to four SPI controllers, each SPI controller with two CS signals
  - Full-duplex synchronous serial interface
  - 1-, or 2-wire mode
- **UART**
  - Up to 8 UART controllers
  - UART0 with 2 wires for debug tools
  - UART1 with 8 wires
  - UART2/3 each with 4 wires
  - Others with 2 wires
  - Compatible with industry-standard 16550 UARTs
- **PS2**
  - Two PS2 controllers
  - Compliant with IBM PS2 and AT-compatible keyboard and mouse interface
  - Dual-role controller:PS2 host or PS2 device
- **CIR**
  - Two CIR controllers
  - Flexible receiver for consumer IR remote control
- **SATA**

- One SATA host controller
- Support SATA 1.5Gb/s and SATA 3.0Gb/s

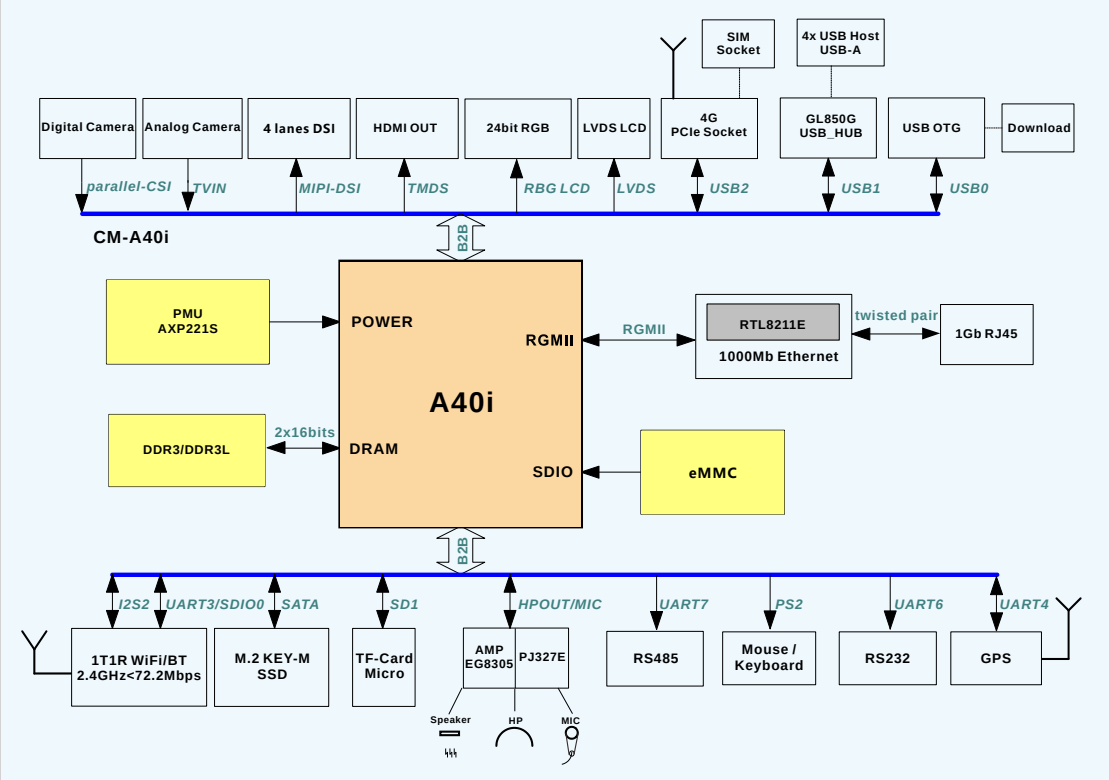
- **Keypad**
  - One keypad matrix interface up to 8 rows and 8 columns
  - Interrupt for key pressor key release
- **KEYADC**
  - Up to two ADC channels for key application
  - 6-bit resolution
  - Voltage input range between 0V to 2V
  - Support ingle, normal and continuous mode
- **PWM**
  - 6 on-chip PWMs (**4** PWM pairs) with interrupt-based operation
  - up to 24/100MHz output frequency
  - Minimum resolution is 1/65536
- **WatchDog**
  - One watchdog to generate reset signal or interrupt
- **Interrupt Controller**
  - Support **32** interrupts
- **3D Graphics Engine**
  - ARM Mali400 MP2 supply
  - Support OpenGL ES 2.0, OpenGL ES 1.1, Open VG 1.1 standard
- **Power unit**
  - AXP221S on board
  - Lion-Battery Charge Management
  - OVP/UVP/OTP/OCP protections
  - Charging current can reach 2.2A
  - Very low RTC consume current, less 5uA at 3V button Cell
- **Temperature**
  - Industrial grade, Operating temperature: -20 - 85°C

1.3 A40i Block Diagram

1.3.1 A40i Block Diagram



1.3.2 Development board (EMA40I) Block Diagram

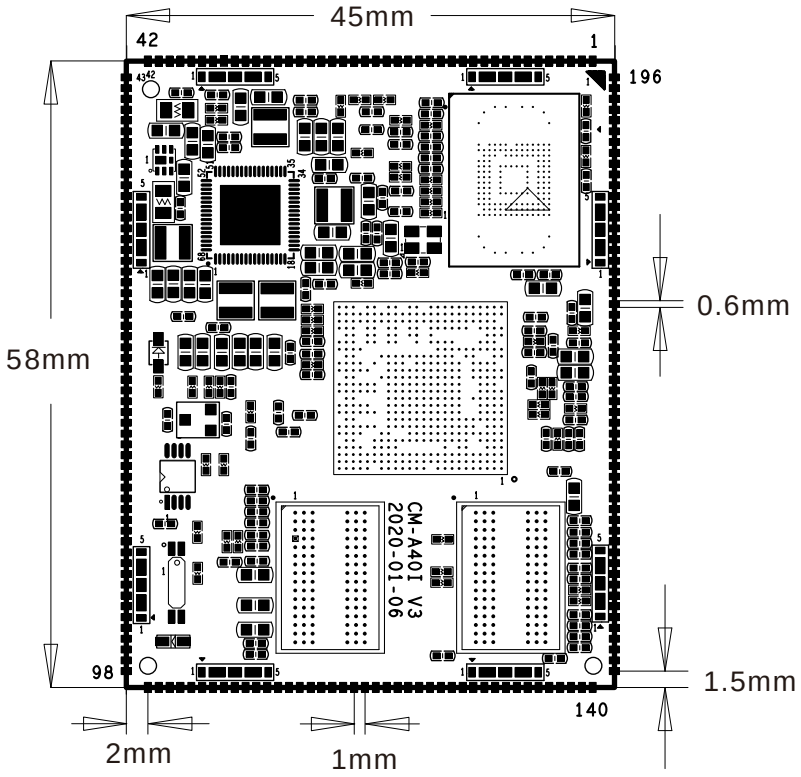


1.4 CM-A40i specifications

Feature	Specifications
CPU	Quad-core Cortex-A7
DDR	1GB DDR3/DDR3L (up to 2GB)
eMMC FLASH	4GB (up to 32GB)
Power	DC 5V or 3.7V Battery
LVDS	Dual CH up to 4-Lane
I2S	1-CH
MIPI_TX	1-CH
SATA	1-CH
HDMI out	1-CH
Camera	1-CH(DVP) and 4-CH(CVBS)
USB	2-CH (USB HOST2.0), 1-CH(OTG 2.0)
Ethernet	1000M GMAC If GMAC is not needed, it can be designed to UARTs and SPIs.
SDMMC	2-CH
SPDIF TX	1-CH
I2C	3-CH

SPI	4-CH
UART	7-CH, 1-CH(DEBUG)
PWM	6-CH
ADC IN	2-CH
Board Dimension	45 x 58mm

1.5 CM-A40i PCB Dimension



1.6 CM-A40i Pin Definition

Pin	Signal	Description	Alternate functions	IO Voltage
1	KEYADC1	6bit ADC channel1		3.3V
2	KEYADC0	6bit ADC channel0		3.3V
3	FEL	Boot mode select: Low: download from USB, High: fast boot		3.3V
4	PD26/LCD0_HSYNC	LCD0 horizontal sync	GPIOD26/SMC_SLK	3.3V
5	PD27/LCD0_VSYNC	LCD0 vertical sync	GPIOD27/SMC_SDA	3.3V
6	USB-DP2	USB2 data +		3.3V

7	USB-DM2	USB2 data -		3.3V
8	USB-DP1	USB1 data +		3.3V
9	USB-DM1	USB1 data -		3.3V
10	USB-DP0	USB0 data +		3.3V
11	USB-DM0	USB0 data -		3.3V
12	PI4/SDC3_CMD	SDC3 command signal	GPIOI4	3.3V
13	HTXCN	HDMI Clock -		1.8V
14	HTXCP	HDMI Clock +		1.8V
15	HTX0N	HDMI output data0-		1.8V
16	HTX0P	HDMI output data0+		1.8V
17	HTX1P	HDMI output data1+		1.8V
18	HTX1N	HDMI output data1-		1.8V
19	HTX2P	HDMI output data2+		1.8V
20	HTX2N	HDMI output data2-		1.8V
21	GND	Ground		0V
22	SATA-RXP	SATA input data+		2.5V
23	SATA-RXM	SATA input data-		2.5V
24	SATA-TXM	SATA output data-		2.5V
25	SATA-TXP	SATA output data+		2.5V
26	HHPD	HDMI hot plug detect		3.3V
27	HSDA	HDMI serial data(Need pull H)		3.3V
28	HSCL	HDMI serial clock(Need pull H)		3.3V
29	HCEC	HDMI consumer electronics control		3.3V
30	PC1/SPI0_MISO	SPI0 master data in, slave data out	GPIOC1	3.3V
31	PC2/SPI0_CLK	SPI0 clock signal	GPIOC2	3.3V
32	PC0/SPI0_MOSI	SPI0 master data out, slave data in	GPIOC0	3.3V
33	PC23/SPI0_CS0	SPI0 chip select signal 0(active low)	GPIOC23	3.3V
34	VCC_IO	Power 3.3V output(500mA limit)		3.3V
35	PF4/SDC0-D3	SDC0 DATA3	GPIOF4	3.3V
36	PF5/SDC0-D2	SDC0 DATA2	GPIOF5	3.3V
37	PF0/SDC0-D1	SDC0 DATA1	GPIOF0	3.3V
38	PF1/SDC0-D0	SDC0 DATA0	GPIOF1	3.3V
39	PF3/SDC0-CMD	SDC0 command signal	GPIOF3	3.3V
40	PF2/SDC0-CLK	SDC0 clock	GPIOF2	3.3V
41	RESET	System RESETn	For WD used	3.3V
42	BAT_TS	Battery temperature sensor input		3.5~4.2V
43	VBAT	Battery power input		3.5~4.2V
44	VBAT	Battery power input		3.5~4.2V
45	GND	Ground		0V

46	GND	Ground		0V
47	USBVBUS	USB VBUS power input		5V
48	VSYS	System power input 5V		4~5V
49	VSYS	System power input 5V		4~5V
50	PE1/CSI0_MLCK	CSI0 master clock output	GPIOE1	3.3V
51	PE2/CSI0_HSYNC	CSI0 horizontal sync	GPIOE2	3.3V
52	PE3/CSI0_VSYNC	CSI0 vertical sync	GPIOE3	3.3V
53	PE0/CSI0_PCLK	CSI0 pixel clock input	GPIOE0	3.3V
54	PE11/CSI0_D7	CSI0 DATA7	GPIOE11	3.3V
55	PE10/CSI0_D6	CSI0 DATA6	GPIOE10	3.3V
56	PE9/CSI0_D5	CSI0 DATA5	GPIOE9	3.3V
57	PE8/CSI0_D4	CSI0 DATA4	GPIOE8	3.3V
58	PE7CSI0_D3	CSI0 DATA3	GPIOE7	3.3V
59	PE6/CSI0_D2	CSI0 DATA2	GPIOE6	3.3V
60	PE5/CSI0_D1	CSI0 DATA1	GPIOE5	3.3V
61	PE4/CSI0_D0	CSI0 DATA0	GPIOE4	3.3V
62	PG3/CSI1_VSYNC		GPIOG3	3.3V
63	PG2/CSI1_HSYNC		GPIOG2	3.3V
64	PG0/CSI1_PCLK		GPIOG0	3.3V
65	PG1/CSI1_MLCK		GPIOG1	3.3V
66	PI13/UART6_RX	UART6 input data	GPIOI13	3.3V
67	PI12/UART6_TX	UART6 output data	GPIOI12	3.3V
68	PI11/UART5_RX	UART5 input data	GPIOI11	3.3V
69	PI10/UART5_TX	UART5 output data	GPIOI10	3.3V
70	PI16/SPI1_CS0	SPI1 chip select signal(active low)	GPIOI16	3.3V
71	PI14/EINT26	SPI0 chip select signal 1(active low)	GPIOI14	3.3V
72	PI17/SPI1_CLK	SPI1 clock signal	GPIOI17	3.3V
73	PI18/SPI1_MOSI	SPI1 master data out, slave data in	GPIOI18	3.3V
74	PI19/SPI1_MISO	SPI1 master data in, slave data out	GPIOI19	3.3V
75	PI20/UART7_TX/PWM2	UART7 output data or PS2_CLK0	GPIOI20/PWM2	3.3V
76	PI21/UART7_RX/PWM3	UART7 intput data or PS2_DAT0	GPIOI21/PWM3	3.3V
77	VCC-RTC	RTC power output		1.8V~3.3V
78	RTC_CLKOUT	RTC clock(32.768khz) output		3.3V
79	POWER-KEY	Power on-off key input(active low)		3.3V
80	PI2/TWI4-SCK	I2C4 clock(Pull H 2K)	GPIOI2	3.3V
81	PI3/TWI4-SDA	I2C4 data(Pull H 2K)	GPIOI3	3.3V

82	PA17/ETXERR/I2S1_DI	MII ETXERR signal	GPIOA17 /I2S1_DI	3.3V
83	GCLKIN/PA16/ECOL/I2S1_DO	RGMII reference clock input(125Mhz)	GPIOA16/I2S1_DO/ECOL	3.3V
84	PA14/ETXCK/UART7_TX/I2S1_BCLK	MII transmit clock	UART7/I2S1 bit clock	3.3V
85	GTXCK	RGMII transmit clock	PA15/ECRS/UART7_RX/I2S1_LRCK	3.3V
86	GRXCK	RGMII receive clock or SPI3_MISO	ERXCK/SPI3_MISO/GPIOA8	3.3V
87	GMDIO	RGMII management data input/output	UART6_TX/7UART1_RTS/GPIOA12	3.3V
88	GMDC	RGMII management data clock	UART1_RX/GPIOA11	3.3V
89	GRXD3	RGMII receive data3	UART2_RTS/SPI1_CS0/GPIOA0	3.3V
90	GRXD2	RGMII receive data2	UART2_CTS/SPI1_CLK/GPIOA1	3.3V
91	GRXD1	RGMII receive data1	UART2_TX/SPI1_MOSI/GPIOA2	3.3V
92	GRXD0	RGMII receive data0	UART2_RX/SIP1_MISO/GPIOA3	3.3V
93	GRXDV	RGMII receive control	UART1_TX/GPIOA10	3.3V
94	GTXD3	RGMII transmit data3	SPI1_CS1/GPIOA3	3.3V
95	GTXD2	RGMII TX data2 or SPI3CS0	SPI3_CS0/GPIOA5	3.3V
96	GTXD1	RGMII TX data1 or SPI3CLK	SPI3_CLK/GPIOA6	3.3V
97	GTXD0	RGMII TX data0 or SPI3MOSI	SPI3_MOSI/GPIOA7	3.3V
98	GTXEN	RGMII transmit control	UART6_RX/UART1_CTS/GPIOA13	3.3V
99	PB15/SPI2_CLK	SPI2 clock signal	GPIOB15/JTAG_CK0	3.3V
100	PB14/SPI2_CS0	SPI2 chip select signal(active low)	GPIOB14/JTAG_MS0	3.3V
101	PB17/SPI2_MISO	SPI2 master data in, slave data out	GPIOB17/JTAG_DI0	3.3V
102	PB16/SPI2_MOSI	SPI1 master data out, slave data in	GPIOB16/JTAG_DO0	3.3V
103	PB19/TWI1_SDA	I2C1_data(Need pull H)	GPIOB19	3.3V
104	PB18/TWI1_SCK	I2C1_clock(Need pull H)	GPIOB18	3.3V
105	PB20/TWI2_SCK/PWM4	I2C2 clock(Need pull H)	GPIOB20/PWM4	3.3V
106	PB21/TWI2_SDA/PWM5	I2C2 data(Need pull H)	GPIOB21/PWM5	3.3V
107	PH20/EINT20		GPIOH20(INT)/LCD1	3.3V

			_D20/CSI1_D20	
108	PH21/EINT21		GPIOH21(INT)/LCD1_D21	3.3V
109	PH19/EINT19/KP_OUT1	SD1 detect signal(Need pull H)	GPIOH19(INT)/KP_OUT1	3.3V
110	PB3/PWM1	PWM1 output	GPIOB3	3.3V
111	PB2/PWM0	PWM0 output	GPIOB2	3.3V
112	PB4/IR0_RX	IR data input (Need pull H)	GPIOB4	3.3V
113	PB8/I2S_DO0	I2S data0 output	GPIOB8	3.3V
114	PB9/I2S_DO1	I2S data1 output	GPIOB9	3.3V
115	PB10/I2S_DO2	I2S data2 output	GPIOB10	3.3V
116	PB11/I2S_DO3	I2S data3 output	GPIOB11	3.3V
117	PB6/I2S_BCLK	I2S bit clock	GPIOB6	3.3V
118	PB7/I2S_LRCK	I2S left/right channel select clock	GPIOB7	3.3V
119	PB12/I2S_DI	I2S data3 input	GPIOB12/SPDIF_DO	3.3V
120	PB5/I2S_MCLK	I2S master clock	GPIOB5	3.3V
121	GND	Ground		0V
122	PB13/SPDIF_DO	SPDIF data output	SPI2_CS1/GPIOB13	3.3V
123	PH12/EINT12	TOUCH_INT	PS2_SCK1/CSI1_D12/LCD1_D12/GPIOH12(INT)	3.3V
124	PH13/EINT13	GPIOH13(INT)	PS2_SDA1/CSI1_D13/SMC_RST/LCD1_D13/GPIOH13	3.3V
125	PH7/EINT7	GPIOH7(INT)	CSI1_D7/MS_CLK/UART5_RX/LCD1_D7/GPIOH7	3.3V
126	PH6/EINT6	LCD back-light enable control	CSI1_D6/MS_BS/UART5_TX/LCD1_D6/GPIOH6	3.3V
127	PH5/UART4_RX/EINT5	UART4 receive	CSI1_D6/LCD1_D5/GPIOH5(INT)	3.3V
128	PH4/UART4_TX/EINT4	UART4 transmit	CSI1_D4/LCD1_D4/GPIOH4(INT)	3.3V
129	PH3/UART3_CTS/EINT3	UART3 CTS(Clear To Send)	CSI1_D3/LCD1_D3/GPIOH3(INT)	3.3V
130	PH2/UART3_RTS/EINT2	UART3 RTS(Require To Send)	CSI1_D2/LCD1_D2/GPIOH2(INT)	3.3V
131	PH1/UART3_RX/EINT1	UART3 receive	CSI1_D1/LCD1_D1/GPIOH1(INT)	3.3V
132	PH0/UART3_TX/EINT0	UART transmit	CSI1_D0/LCD1_D0/GPIOH0(INT)	3.3V
133	PB23/UART0_RX	UART0 receive (for debug)	IR1_RX/GPIOH23(IN	3.3V

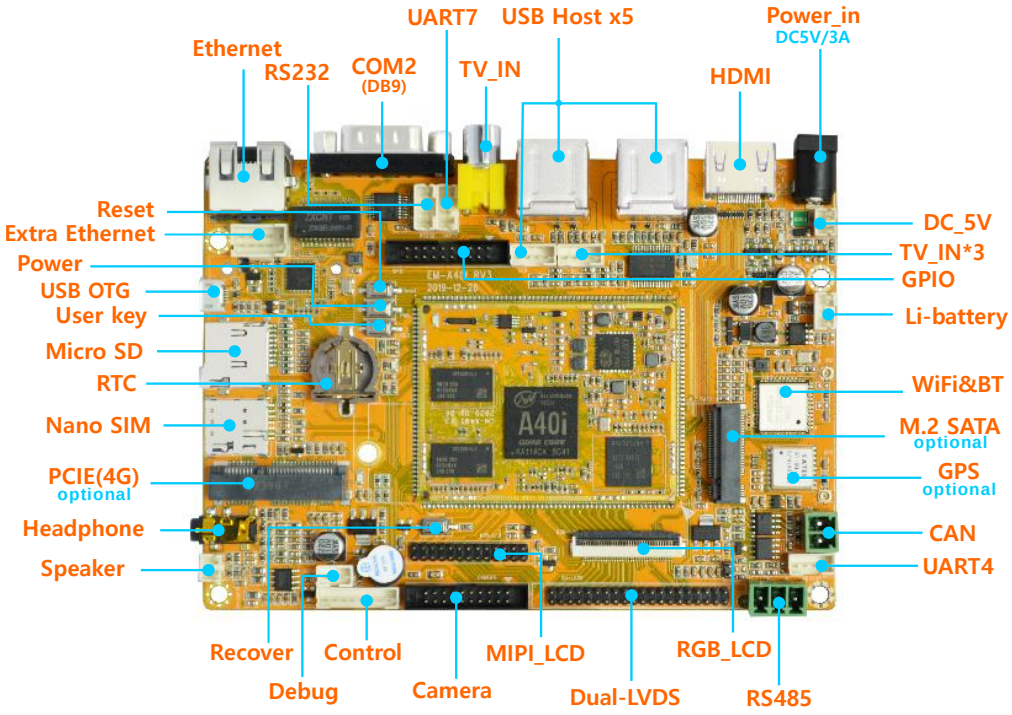
			T)	
134	PB22/UART0_TX	UART0 transmit (for debug)	GPIOH22(INT)	3.3V
135	PH8/EINT8/KP_IN0	GPIOH8(INT)	CSI1_D8/MS_D0/KP_IN0/LCD1_D8	3.3V
136	PH9/EINT9/KP_IN1	GPIOH9(INT)	CIS1_D9/MS_D1/KP_IN1/LCD1_D9	3.3V
137	PH16/EINT16/KP_IN6	GPIOH16(INT)	CSI1_D16/SMC_DET/KP_IN6/LCD1_D16	3.3V
138	PH11/EINT11/KP_IN3	GPIOP11(INT)	CSI1_D11/MS_D3/KP_IN3/LCD1_D11	3.3V
139	PH10/EINT10/KP_IN2	GPIOH10(INT)	CSI1_D10/MS_D2/KP_IN2/LCD1_D10	3.3V
140	PH14/EINT14/KP_IN4	GPIOH14(INT)	CSI1_D14/SMC_VPPEN/KP_IN4/LCD1_D14	3.3V
141	PH15/EINT15/KP_IN5	GPIOH15(INT)	CSI1_D15/SMC_VPPPP/KP_IN5/LCD1_D15	3.3V
142	PH17/EINT17/KP_IN7	GPIOH17(INT)	CSI1_D17/SMC_VCCEN/KP_IN7/LCD1_D17	3.3V
143	PH18/EINT18/KP_OUT0	GPIOH18(INT)	CSI1_D18/SMC_SLK/KP_OUT0/LCD1_D18	3.3V
144	PH23/SDC1_CLK	SDC1 clock	CSI1_D23/KP_OUT3/LCD1_D23/GPIOH23	3.3V
145	PH27/SDC1_D3	SDC1 data3	CSI1_VSYNC/KP_OUT7/LCD1_VSYNC/GPIOH27	3.3V
146	PH26/SDC1_D2	SDC1 data2	CSI1_HSYNC/KP_OUT6/LCD1_HSYNC/GPIOH26	3.3V
147	PH25/SDC1_D1	SDC1 data1	CSI1_FIELD/KP_OUT5/LCD1_DE/GPIOH25	3.3V
148	PH24/SDC1_D0	SDC1 data0	CSI1_PCLK/KP_OUT4/LCD1_CLK/GPIOH24	3.3V
149	PH22/SDC1_CMD	SDC1 command signal	CSI1_D22/KP_OUT2/LCD1_D22/GPIOH22	3.3V
150	GND	Ground		0V

151	MIPI-DSI-D3N	MIPI DSI differential data3 negative		3.3V
152	MIPI-DSI-D3P	MIPI DSI differential data3 positive		3.3V
153	MIPI-DSI-D2N	MIPI DSI differential data2 negative		3.3V
154	MIPI-DSI-D2P	MIPI DSI differential data2 positive		3.3V
155	MIPI-DSI-D1N	MIPI DSI differential data1 negative		3.3V
156	MIPI-DSI-D1P	MIPI DSI differential data1 positive		3.3V
157	MIPI-DSI-D0N	MIPI DSI differential data0 negative		3.3V
158	MIPI-DSI-D0P	MIPI DSI differential data0 positive		3.3V
159	MIPI-DSI-CKN	MIPI DSI differential clock negative		3.3V
160	MIPI-DSI-CKP	MIPI DSI differential clock positive		3.3V
161	PD20/LCD0_D20	LCD0 data20	CSI1_MCLK/GPIOD20	3.3V
162	PD21/LCD0_D21	LCD0 data21	SMC_VPPEN/GPIOD21	3.3V
163	PD22/LCD0_D22	LCD0 data22	SMC_VPPPP/GPIOD22	3.3V
164	PD23/LCD0_D23	LCD0 data23	SMC_DET/GPIOD23	3.3V
165	PD24/LCD0_CLK	LCD0 clock	SMC_VCCEN/GPIOD24	3.3V
166	PD25/LCD0_DE	LCD0 data enable	SMC_RST/GPIOD25	3.3V
167	PD0/LVDS0_VP0/LCD0_D0	LCD0 data0/LVDS0 data0 positive signal output((only one function work at same time)	GPIOD0	3.3V
168	PD1/LVDS0_VN0/LCD0_D1	LCD0 data1/LVDS0 data0 negative signal output((only one function work at same time)	GPIOD1	3.3V
169	PD2/LVDS0_VP1/LCD0_D2	LCD0 data2/LVDS0 data1 positive signal output((only one function work at same time)	GPIOD2	3.3V
170	PD3/LVDS0_VN1//LCD0_D3	LCD0 data3/LVDS0 data1 negative signal output((only one function work at same time)	GPIOD3	3.3V
171	PD4/LVDS0_VP2/LCD0_D4	LCD0 data4/LVDS0 data2 positive signal output((only one	GPIOD4	3.3V

		function work at same time)		
172	PD5/LVDS0_VN2/LCD0_D5	LCD0 data5/LVDS0 data2 negative signal output((only one function work at same time)	GPIOD5	3.3V
173	PD6/LVDS0_VPC//LCD0_D6	LCD0 data6/LVDS0 clock positive signal output((only one function work at same time)	GPIOD6	3.3V
174	PD7/LVDS0_VNC//LCD0_D7	LCD0 data7/LVDS0 clock negative signal output((only one function work at same time)	GPIOD7	3.3V
175	PD8/LVDS0_VP3//LCD0_D8	LCD0 data8/LVDS0 data3 positive signal output((only one function work at same time)	GPIOD8	3.3V
176	PD9/LVDS0_VN3//LCD0_D9	LCD0 data9/LVDS0 data3 negative signal output((only one function work at same time)	GPIOD9	3.3V
177	PD10/LVDS1_VP0/LCD0_D10	LCD0 data10/LVDS1 data0 positive signal output((only one function work at same time)	GPIOD10	3.3V
178	PD11/LVDS1_VN0/LCD0_D11	LCD0 data11/LVDS1 data0 negative signal output((only one function work at same time)	GPIOD11	3.3V
179	PD12/LVDS1_VP1/LCD0_D12	LCD0 data12/LVDS1 data1 positive signal output((only one function work at same time)	GPIOD12	3.3V
180	PD13/LVDS1_VN1/ LCD0_D13	LCD0 data13/LVDS1 data1 negative signal output((only one function work at same time)	GPIOD13	3.3V
181	PD14/LVDS1_VP2/LCD0_D14	LCD0 data14/LVDS1 data2 positive signal output((only one function work at same time)	GPIOD14	3.3V
182	PD15/LVDS1_VN2/ LCD0_D15	LCD0 data15/LVDS1 data2 negative signal output((only one function work at same time)	GPIOD15	3.3V
183	PD16/LVDS1_VPC/ LCD0_D16	LCD0 data16/LVDS1 clock positive signal output((only one function work at same time)	GPIOD16	3.3V
184	PD17/LVDS1_VNC/ LCD0_D17	LCD0 data17/LVDS1 clock negative signal output((only one function work at same time)	GPIOD17	3.3V
185	PD18/LVDS1_VP3/LCD0_D18	LCD0 data18/LVDS1 data3 positive signal output((only one function work at same time)	GPIOD18	3.3V
186	PD19/LVDS1_VN3/	LCD0 data19/LVDS1 data3	GPIOD19	3.3V

	LCD0_D19	negative signal output((only one function work at same time)		
187	HPOUTR	Headphone right channel output		0V
188	HPOUTL	Headphone left channel output		0V
189	AGND	Audio analog ground		0V
190	MICIN1	microphone input1		0V
191	VMIC	Bias voltage output for main microphone		3.3V
192	GND-TVIN	CVBS-IN analog ground		0V
193	TVIN0	CVBS input0	YUV input	0V
194	TVIN1	CVBS input1	When TVIN0 input YUV, this pin can't be used	0V
195	TVIN2	CVBS input2	When TVIN0 input YUV, this pin can't be used	0V
196	TVIN3	CVBS input3		0V
Note *GPIOx(INT) or EINTx means the pin has interrupt function.*				

1.7 Development Kit (EMA40I)

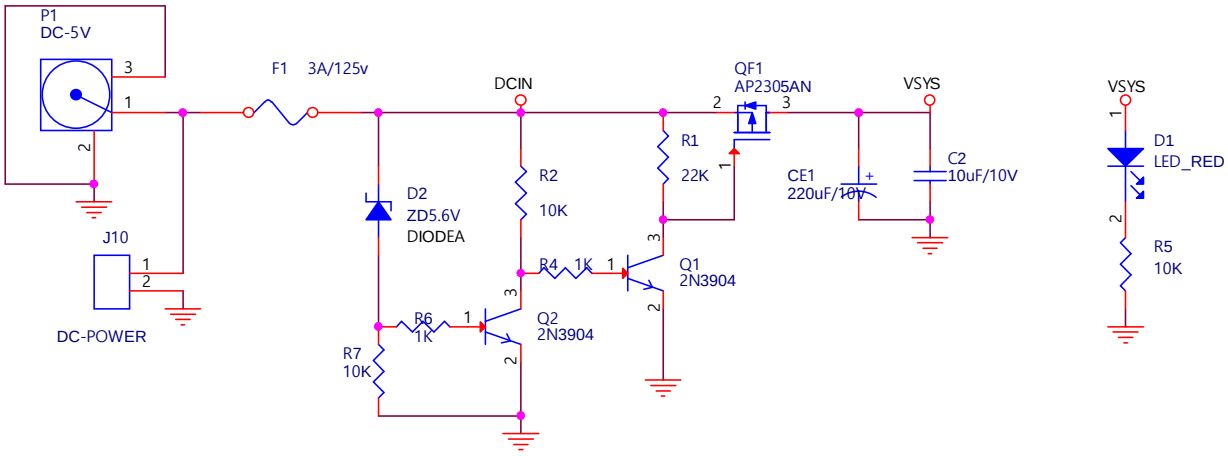


2 Hardware Design Guide

2.1 Peripheral Circuit Reference

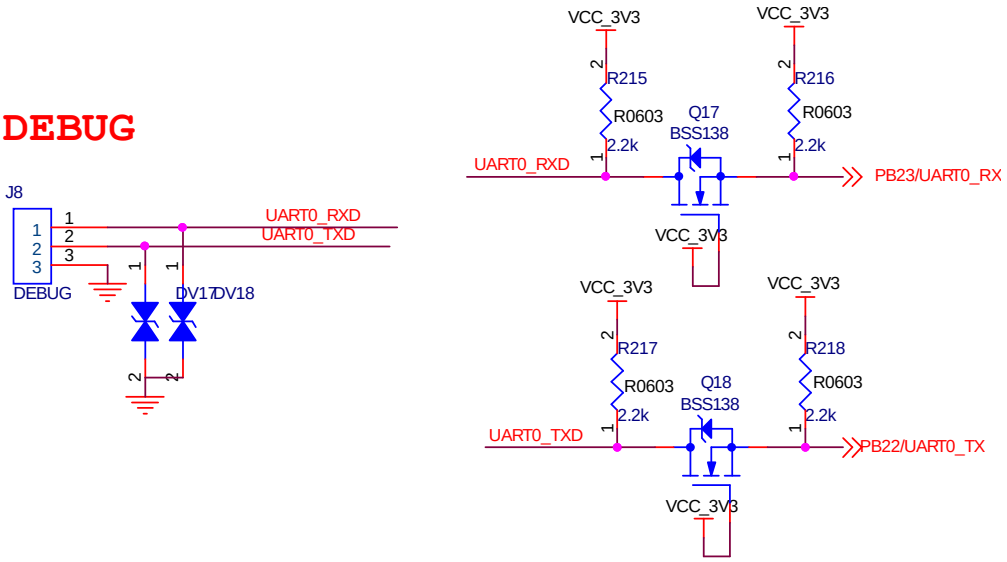
2.1.1 External Power

MAIN 5V

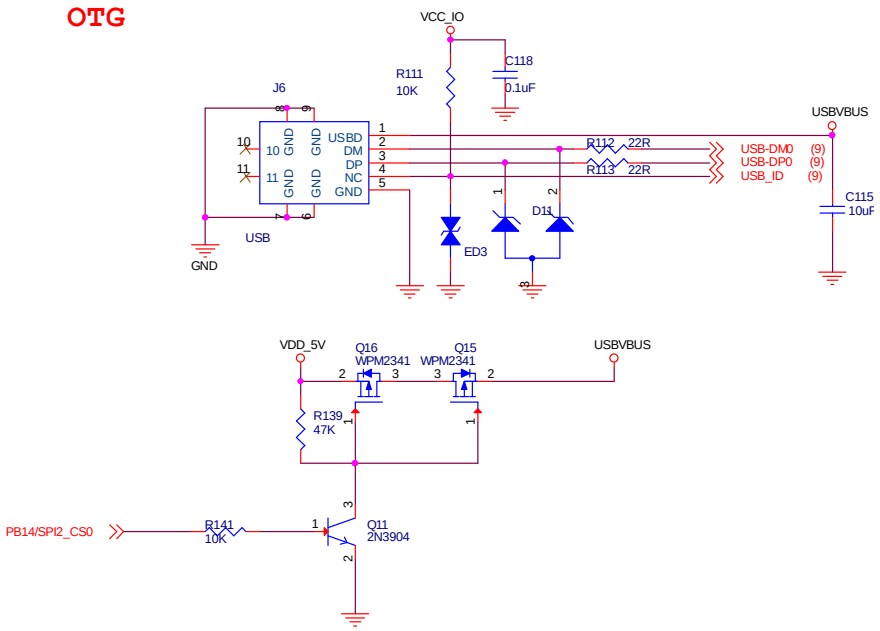


2.1.2 Debug Circuit

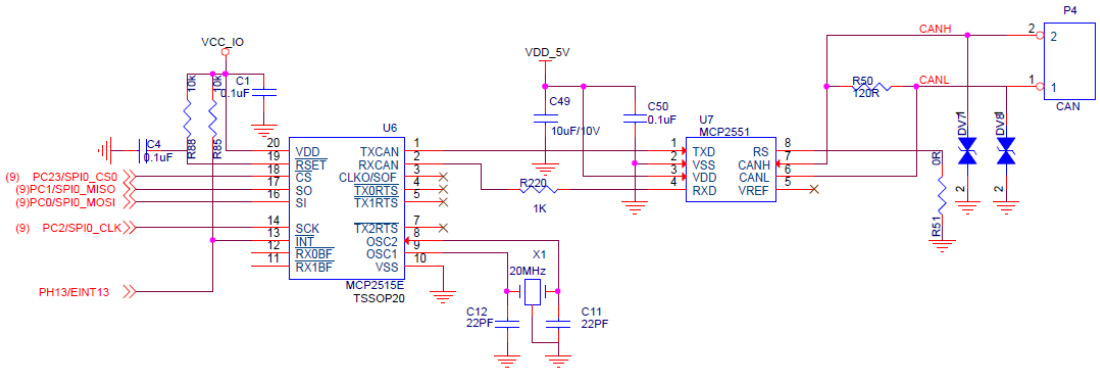
DEBUG



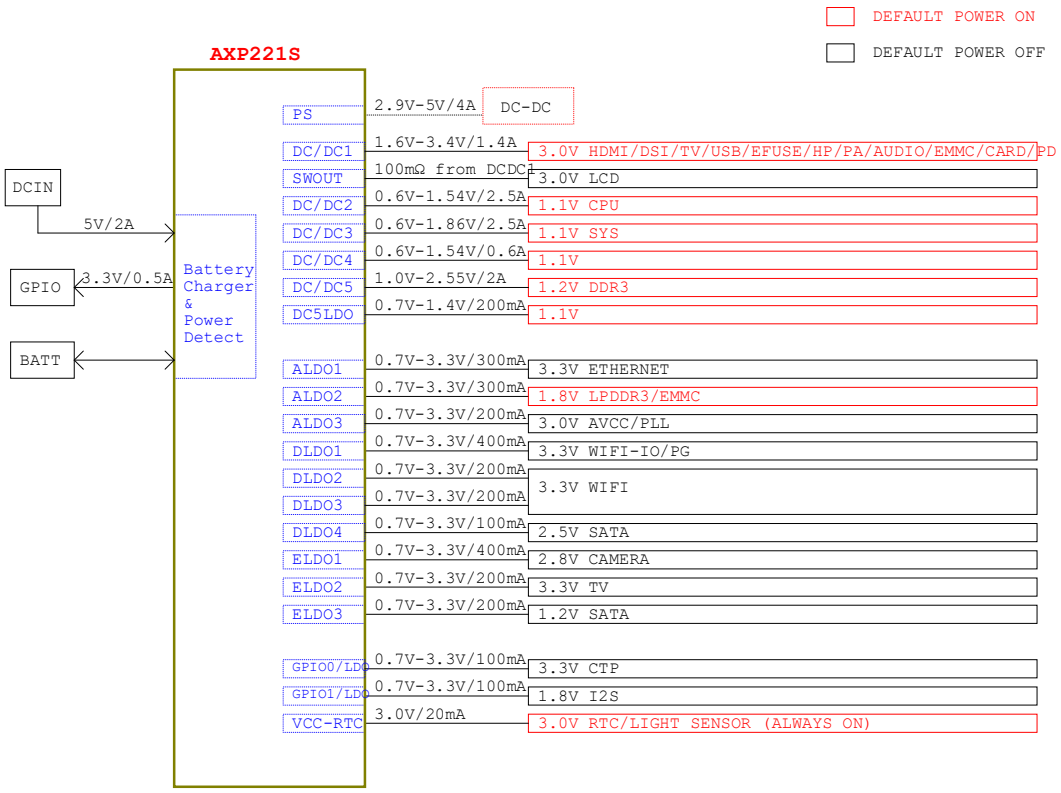
2.1.3 USB OTG Interface Circuit



2.1.4 CAN Interface Circuit



2.2 Power Tree



3 Product Electrical Characteristics

3.1 Dissipation and Temperature

Symbol	Parameter	Min	Typ	Max	Unit
VSYS	System Voltage	3.8	5	6	V
VCC_IO	System IO Voltage	3.3-5%	3.3	3.3+5%	V
Isys_in	VSYS input Current		800	1600	mA
Ivio_out	VCC_IO output Current		400	500	mA
VCC_RTC	RTC Voltage	1.8	3	3.4	V
Iirtc	RTC input Current		5	8	uA

Ta	Operating Temperature	-20		70	°C
Tstg	Storage Temperature	-40		85	°C

3.2 Reliability of Test

High Temperature Operating Test		
Contents	Operating 8h in high temperature	55°C±2°C
Result	Pass	

Operating Life Test		
Contents	Operating in room	120h
Result	Pass	