Rockchip RV1126B-P Datasheet

Revision 1.0
May 2025

Revision History

Date	Revision	Description
2025-05-22	1.0	Initial release

Table of Content

Table of Content 3
Figure Index 4
Table Index 5
Warranty Disclaimer 6
Chapter 1 Introduction 7
1.1 Overview 7
1.2 Features 7
1.3 Block Diagram 17
Chapter 2 Package Information 19
2.1 Order Information 19
2.2 Top Marking 19
2.3 Package Dimension 20
2.4 MSL Information 21
2.5 Lead Finish/Ball material Information 21
2.6 Pin Number List 21
2.7 IO Pin Name Description 28
Chapter 3 Electrical Specification 33
3.1 Absolute Ratings 33
3.2 Recommended Operating Condition 33
3.3 DC Characteristics 34
3.4 Electrical Characteristics for General IO 35
3.5 Electrical Characteristics for PLL 36
3.6 Electrical Characteristics for USB2.0 Interface 36
3.7 Electrical Characteristics for DDR IO 37
3.8 Electrical Characteristics for MIPI DSI 37
3.9 Electrical Characteristics for MIPI CSI interface 37
3.10 Electrical Characteristics for SARADC 37
3.11 Electrical Characteristics for TSADC 38
Chapter 4 Thermal Management 39
4.1 Overview 39
4.2 Package Thermal Characteristics 39

Figure Index

Fig. 1-1 Block Diagram 18
Fig. 2-1 RV1126B-P Package Top and Side View 20
Fig. 2-2 RV1126B-P Package Bottom View 20
Fig. 2-3 RV1126B-P Package Dimension 21

Table Index

Table 2-1 RV1126B-P Pin Number Order Information 21
Table 2-2 IO function description list 28
Table 3-1 Absolute ratings.....33
Table 3-2 Recommended operating condition 33
Table 3-3 DC Characteristics.....34
Table 3-4 Electrical Characteristics for Digital General IO 35
Table 3-5 Electrical Characteristics for INT PLL 36
Table 3-6 Electrical Characteristics for FRAC PLL.....36
Table 3-7 Electrical Characteristics for USB2.0 Interface 36
Table 3-8 Electrical Characteristics for DDR IO 37
Table 3-9 Electrical Characteristics for MIPI DSI 37
Table 3-10 HS Receiver AC specifications (for MIPI mode) 37
Table 3-11 LP Receiver AC specifications (for MIPI mode) 37
Table 3-12 HS Receiver AC specifications (for LVDS mode) 37
Table 3-13 Electrical Characteristics for SARADC 37
Table 3-14 Electrical Characteristics for TSADC 38
Table 4-1 Thermal Resistance Characteristics.....39

Warranty Disclaimer

Trademark

Rockchip is a registered trademark of Rockchip Electronics Co., Ltd. in the People's Republic of China and other countries/areas. Other brands, product names mentioned in this document are the property of their respective owners.

Disclaimer

Rockchip Electronics Co., Ltd. ("Rockchip") may make changes to any information in this document at any time without any prior notice.
Information in this document is provided just as a reference or typical applications. All or part of product features described in this document may not be within the purchase scope or the usage scope, and may be subject to the third party licensing requirements. All statements, information in this document is provided "AS IS" without warranties of any kind, either express or implied. Actual performance of Rockchip products may vary in different applications. Third party licenses maybe required to use some features supported by Rockchip products. Customers shall be solely and exclusively responsible to obtain all appropriately required third party licenses prior to its such use. Should customers use the features supported by Rockchip products without any required third party license, customers shall indemnify and hold Rockchip and its subsidiaries, affiliates as well as distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of any claim associated with such unauthorized use.
Rockchip products are not intended for use in military, airplane, medical devices, lifesaving or life sustaining applications ("Unintended Uses"). Customers shall take any and all actions to ensure using Rockchip products in a lawful manner and shall be liable for Unintended Uses.

Chapter 1 Introduction

1.1 Overview

RV1126B-P is a high-performance vision processor SoC for machine vision application, especially for AI related application.

It is based on quad-core ARM Cortex-A53 64-bit core which integrates NEON and FPU. There is a 32KB I-cache and 32KB D-cache for each core and 512KB unified L2 cache.
The build-in NPU Support INT8/INT16 hybrid operation and computing power is up to 3.0TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RV1126B-P introduces a new generation totally hardware-based maximum 12-Megapixel ISP (image signal processor) and post processor. It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, fisheye correction, gamma correction, feature points detection and so on. A maximum 8-Megapixel AI-ISP is also introduced as a complement to traditional ISP, which offers superior spatial denoising performance and enhanced image enhancement effects. Cooperating with two MIPI CSI(or LVDS/SubLVDS) and one DVP(BT.601/BT.656/BT.1120) interface, users can build a system that receives video data from four camera sensors simultaneously.

The video encoder embedded in RV1126B-P support H.265/H.264 video encoding and the multi-stream encoding is supported also. With the help of this feature, the video from camera can be encoded with higher resolution and stored in local memory and transferred another lower resolution video to cloud storage at the same time.

The H.264/H.265 video decoder in RV1126B-P support 4Kp30 for H.264 and H.265.
In addition to the previous high-performance multimedia block, RV1126B-P also contains rich audio, memory and other peripheral interfaces such as I2C, SPI, PWM and so on. These can help users add more sensors or other peripherals into whole system to improve flexibility and expansibility.

RV1126B-P has high-performance external DRAM(DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/4X) capable of sustaining demanding memory bandwidths.

1.2 Features

1.2.1 Application Processor

- Quad core ARM Cortex-A53
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD
- Separately Integrated Neon and FPU
- 32KB L1 I-Cache and 32KB L1 D-Cache
- Unified 512KB L2 Cache for Cortex-A53
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_CPU2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache
  - PD_CPU3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - Bootrom
    - Support system boot from the following device:
      - SPI interface
      - eMMC interface
      - SD/MMC interface

- Support system code download by the following interface:
  - USB2.0 interface
  - UART interface
- 64KB system SRAM
- 8KB PMU SRAM

- External off-chip memory
  - Dynamic Memory Interface (DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X)
    - Compatible with JEDEC standards
    - Compatible with DDR3/DDR3L/ DDR4 /LPDDR3/LPDDR4/LPDDR4X
    - Support 32-bit data width, 2 ranks (chip selects), max 4GB addressing space per rank, total addressing space is 4GB (max)
    - Low power modes, such as power-down and self-refresh for SDRAM
  - eMMC Interface
    - Fully compliant with JEDEC eMMC 4.51 specification
    - Support HS200, but not support CMD Queue
    - Support three data bus width mode: 1bit, 4bits and 8bits
  - SD/MMC Interface
    - Compatible with SD3.0, MMC ver4.51
    - Support 1bit, 4bits data bus width
  - Flexible Serial Flash Interface (FSPI0)
    - Support transfer data from/to serial flash device
    - Support 1bit, 2bits or 4bits data bus width
    - Support 2 chips select

1.2.3 System Component

- HPMCU
  - Integrated 16KB Cache
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU
  - Integrated Debug Controller with JTAG interface

- CRU (clock & reset unit)
  - Support total 4 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Support 4 separate voltage domains，CPU_DVDD,NPU_DVDD,VDD_LOGIC,VDD_PMU
  - Support 3 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - Support 2 secure timers with 64bits counter and interrupt-based operation
  - Support 6 non-secure timers with 64bits counter and interrupt-based operation
  - Support 1 non-secure timers with 64bits counter for low power mode application
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a

timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Three Watchdog for non-secure application
- One Watchdog for secure application

- Interrupt Controller
  - Support 256 SPI interrupt sources input from different components inside SoC
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive or rising edge sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Support 2 physical channels
  - Support 39 groups of peripheral request interfaces
  - Support 48 logic channels, each logic channel support the following feature
    - Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - Support Linked list DMA function to complete scatter-gather transfer
    - Support three kinds of multi-block transfer: contiguous address, auto reload, link list

- Secure System
  - Support one cipher engine
    - Support Symmetrical algorithms
      - AES-128, AES-192, AES-256, SM4
      - ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES and SM4
    - Hash algorithm
      - SHA-1, SHA-256/224, MD5, SM3 with hardware padding
      - HMAC of SHA-1, SHA-256, MD5, SM3 with hardware padding
    - Asymmetrical algorithms
      - RSA (up to 4096 bits), ECC (up to 256 bits), SM2
    - Key-ladder(KL)
      - Support obtaining the root key from OTP or RKRNG and deriving it
      - Support write out root key or derived key to some specific modules
      - Number of stages can be configured
  - Support secure OTP
  - Support secure debug
  - Support secure OS
  - Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
  - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
  - System SRAM, part of space is addressed only in security mode
  - External DDR space can be divided into 16 parts, each part can be software-programmable to be enabled by each master

- Mailbox
  - One Mailbox with 4 channels in SoC used to service Cortex-A53 and HPMCU communication
  - Support independent interrupt in each Mailbox channel

- Decompression

- Support for decompressing GZIP files
- Support for decompressing data in DEFLATE format
- Support for decompressing data in ZLIB format
- Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

1.2.4 Video CODEC

- Video Decoder
  - Real-time decoding of H.264 and H.265
  - Support MMU
  - H.265 HEVC/MVC Main Profile yuv420@L5.0 up to 3840x2160@30fps
  - H.264 AVC/MVC Main Profile yuv400/yuv420/yuv422@L5.1 up to 3840x2160@30fps
- Video Encoder
  - HEVC Main Profile, Level 5.0 High Tier
  - H.264 High Profile, Level 5.0
  - JPEG Baseline
  - Parallel encoding (HEVC+JPEG or H264+JPEG)
  - Support up to 12M@30fps
  - Support common primary stream such as 3840x2160@30fps, 1920x1080@30fps
  - Bitrate up to 200Mbps with CBR/VBR/FixQP/QPMAP bitrate control
  - YUV420 and YUV400 stream format
  - Slice split
  - Area and block mapping ROI
  - 8-area OSD
  - Link table configuration mode
  - YUV/RGB video source with crop, rotation and mirror
  - Ultra low delay encoding
  - Motion and Occlusion Detection
  - Dual reference frame search(HEVC)
- JPEG Decoder
  - Support Baseline(DCT sequential)
  - Support JPEG file interchange format (JFIF) 1.02
  - Support image size is from 48x48 to 65520x65520
  - Support YUV400/YUV420/YUV422/YUV440/YUV411/YUV444

1.2.5 Neural Process Unit

- Rockchip NPU engine:
  - 3 TOPS* for INT8
  - Support INT4, INT8, INT16, FP16 operation
  - Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

  * Sparsity
- One isolated voltage domain to support DVFS

1.2.6 2D Graphics Engine

- 2D Graphics Engine(RGA)
- Data format
  - SRC0 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - RGB888P/RGB565
    - YUV422-P/YUV422-SP-8bit/10bit(clip to 8bit after input)
    - YUV420-P/YUV420-SP-8bit/10bit(clip to 8bit after input)
    - YUV444I/YUV444SP-8bit
    - YVYU422-8bit
    - YUV400-8bit
    - TILE4X4 YUV420/422/444-8bit
    - TILE4X4 YUV420/422/444-10bit(clip to 8bit after input)

        - BPP1/2/4/8
    - SRC1 Input data format:
        - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
        - RGB888P/RGB565
    - Output data format(all YUV format is 8bit):
        - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
        - RGB888/RGB565
        - YUV420/YUV422 P/SP
        - YUV400/Y4
        - YUV444SP/444I
    - Pixel Format conversion, BT.601/BT.709
    - Dither operation
    - Max resolution: 8192x8192 source, 4096x4096 destination
- Scaling
    - Down-scaling: Average/Bilinear filter
    - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
    - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
    - 0, 90, 180, 270 degree rotation
    - x-mirror, y-mirror operation
    - Mirroring and rotation co-operation
- BitBLT
    - Block transfer
    - Color palette/Color fill, support with alpha
    - Transparency mode (color keying/stencil test, specified value/value range)
    - Two source BitBLT
    - A+B=B only BitBLT, A support rotate & scale when B fixed
    - A+B=C second source (B) has same attribute with (C) plus rotation function
- Alpha Blending
    - Comprehensive per-pixel alpha(color/alpha channel separately)
    - Fading
    - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
    - Support DST Full CSC convert for YUV2YUV
- OSD Automatic Inversion
    - Support OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
    - Support SRC0 and OSD overlay

1.2.7 Display Interface

- Support MCU/RGB LCD Interface up to 24-bits
- Support BT.656/BT.1120 Interface
- Support 4lane MIPI interface, 1.5Gbps/lane
- Max output resolution is 1920x1080@60fps

1.2.8 Video Output Processor (VOP)

- Up to 1920x1080 @60fps
- Multiple layer
    - Background layer
        - programmable 24-bit color
    - Win0 layer
        - YUV444,YUV422,YUV420,RGB888, ARGB888, RGB565
        - Support virtual display
        - 256 level alpha blending (pre-multiplied alpha support)
        - Transparency color key
        - RGB2YUV(BT601_l/BT709_l)
        - YUV2RGB(BT601_l/BT709_l/BT601_f)
    - Win2 layer
        - RGB888, ARGB888, RGB565
        - Support virtual display

- 256 level alpha blending (pre-multiplied alpha support)
- Transparency color key
- RGB2YUV(BT601/BT709)
- Support multi-region

- Support RGB or YUV domain overlay
- BCSH (Brightness, Contrast, Saturation, Hue adjustment)
- BCSH: RGB2YUV (BT601/BT709)
- Support Gamma adjust for PAD
- Support dither down allegro RGB888to666 RGB888to565 and dither down FRC (Frame Rate Control) (configurable) RGB888to666
- Blank and black display
- Standby mode

1.2.9 Video Input Interface

- MIPI Interface
  - Support Two MIPI CSI/LVDS/SubLVDS DPHY
    - Each MIPI DPHY V1.2, 4lanes, 2.5Gbps per lane
    - Support virtual channel
- DVP interface
  - 8/10/12/14/16-bit, up to 150MHz I/O frequency
  - BT.601/BT.656 and BT.1120 VI interface
  - Support the polarity of pixel_clk, hsync, vsync configurable

1.2.10 Image Signal Processor

- Video Capture (VICAP)
  - Support BT.601 RAW8/10/12/14 YCbCr 422 8-bit input
  - Support BT.656 YCbCr 422 8-bit progressive/interlaced input
  - Support 16-pins BT.1120 YCbCr 422 8-bit progressive/interlaced input
  - Support 2/4 mixed BT.656/BT.1120 YCbCr 422 input
  - Support dual-edge sampling for BT.656/BT.1120
  - Support receiving four groups of MIPI CSI/LVDS interfaces, up to four IDs for each group
  - Support VC/DT configurable for each ID
  - Support ten MIPI CSI data formats: RAW8/10/12/14/16, RGB888, YUV422 8bit, YUV422 8bit interlaced, YUV420 8bit, Legacy YUV420 8bit
  - Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
  - Support four LVDS data formats: RAW8/10/12, YUV422 8bit
  - Support RAW rounding
  - Support window cropping
  - Support reducing frame rate
  - Support 4/8/16/32 times down-sampling for RAW data
  - Support RAW 2x2 binning
  - Support pixel extraction from 2x2 pattern
  - Support UV mean down-sampling for YUV422
  - Support compact/non-compact output format for RAW data
  - Support NV16/NV12/YUV400/YUYV output format for YUV data
  - Support virtual stride when write to DDR
  - Support DMA wrap mode
  - Support DMA burst gather 2/4/8
  - Support MMU
  - Support QOS(hurry/press)
  - Support sending RAW data directly to ISP

- Image Signal Process (ISP)
  - VICAP input: RX raw8/raw10/raw12/raw14/raw16
  - Maximum input: 12M@30fps
  - Minimum input: 264x264

- RGBIR: Remosaic RGB-IR pattern to RGB pattern
- Auto Enhance (AE)/Histogram, Auto Focus (AF) and Auto White Balance (AWB) statistics output
- BLC: Black Level Correction
- DPCC: Static/Dynamic Defect Pixel Cluster Correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens Shading Correction
- Bayer-3DNR: Temporal Bayer-raw Noise Reduction
- CAC: Chromatic Aberration Correction
- HDR-MGE: 2-Frame Merge into High-Dynamic Range
- EXPANDER: Sensor expander
- GIC: Green Imbalance Correction
- HDR-DRC: HDR Dynamic Range Compression, tone mapping in RGB filed
- DeBayer: Advanced Adaptive Demosaic
- CCM/CSM: Color Correction Matrix, RGB2YUV
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic dehaze and effect enhancement
- LocalHist: local histogram to enhance local contrast
- HSV: Hue, Saturation,Value color palette for customer
- LDCH: Lens Distortion Correction in the Horizontal direction
- YNR: Spatial luma (Y) Noise Reduction in YUV domain
- CNR: Spatial chroma(C) Noise Reduction in YUV domain
- Sharp: Image sharpening and boundary filtering
- Gain: Image local gain
- Multi-sensor reuse ISP, 2 sensors for maximum
- Bus interface: 32bit AHB configuration, 128bit AXI R/W
- Low power, auto-gating for each block
- MI R/W burst group to improve memory utilization
- MI 2 paths output, MP stepless scaling, SP 1080p (width no more than 1920) scaling
- tile4x4 output
- Online mode: support data from VICAP and data to Encoder, data from ISP to VPSS, ISP to VPSL
- Support ISP2NPU with AI-ISP path, BAY3D output IIR data and gain data to DDR which used by NPU

- AI-ISP
  - Operator modes
    - Mode0: 18x18 convolution
    - Mode1: 24x24 convolution
  - Network Depth
    - Single mode Support up to 8 layers
    - Combo mode Support up to 16 layers
  - Processing Modes
    - Single mode Support up to 6 input channels (commonly 4 channels)
    - Combo mode Support up to 7 input channels
  - Channel Control
    - Each input channel has an independent enable control
    - some input channels support up-sampling and S2D operations
  - Maximum Resolution: Support up to 4096x4096
  - Support maximum 8M@30fps performance

- FishEye Correction(FEC)
  - Input mode and data format
    - RASTER: YUV420SP
    - TILE: YUV420
  - Output mode and data format
    - RASTER: YUV420SP

        - TILE: YUV420
        - FBCE: YUV420
        - QUAD(To AVSP): YUV420
    - Support 32x16,16x8, 4x4(only support 4096x4096 resolution below) density
    - Support up to 4 times reduction factor
    - Input resolution 64x64~8160x8160
    - Output resolution 64x64~8160x8160
    - Performance will be almost 3840x2160 30fps, which different meshgrid will affedct it

- Any View Stitching Processor(AVSP)
    - DCP Input mode and data format
        - RASTER: YUV420SP
        - QUAD: YUV420
    - DCP Output mode and data format
        - RASTER: YUV420SP
        - QUAD: YUV420
    - RCS Input mode and data format
        - QUAD:YUV420
    - RCS Output mode and data format
        - RASTER: YUV420SP
        - TILE: YUV420
        - FBCE:YUV420
    - Support resolution 64x64~1024x4096
    - Support band number 1~6
    - Support decomposition output directly

1.2.11 Video Processing Sub-System(VPSS)

- VPSS
    - Offline DMA input:
        - Line RGB888/ARGB888/RGB565/UYVY/YUV422/YUV420 SP 8bits
        - Tile4x4 YUV422/YUV420 8bits (Rotate 0/90/180/270)
        - RKFBCD64x4 YUV444/YUV422/YUV420 8bits
        - Line-Rot90 UYVY/YUV422/YUV420 8bits (Rotate 90)
    - Online ISP input
    - Both DMA and ISP input
    - Six output channels
    - Maximum image resolution: 4096x3072 (width no more than 4096)
    - Minimum image resolution: 32x32
    - YUV422 processing
    - MIRROR: Horizontal Mirror
    - CMSC: Cover or Mosaic in 8 areas
    - CROP: Cropping on 6 channels
    - Channel0 output:
        - Scale: Bilinear or average filter
        - ASPT_RATIO: Aspect Ratio for image boundary extension
        - Output scan order:
            - Line YUV422/YUV420 SP 8bits
            - Tile4x4 YUV422/YUV420 8bits
            - RKFBCE64x4 YUV422/YUV420 8bits
        - Flip: Vertical Flip for line mode
    - Channel1 output:
        - Scale: Bilinear filter
        - ASPT_RATIO: Aspect Ratio for image boundary extension
        - Output scan order:
            - Line RGB888/ARGB888/RGB565/YUV422/YUV420 SP 8bits
            - Tile4x4 YUV422/YUV420 8bits
            - RKFBCE64x4 YUV422/YUV420 8bits

- Flip: Vertical Flip for line YUV mode
- Resolution up to 12M@30fps

- Channel2 output:
  - Scale: Bilinear or average filter (output width no more than 1920)
  - ASPT_RATIO: Aspect Ratio for image boundary extension
  - Output scan order: Line YUV422/YUV420 SP 8bits
  - Flip: Vertical Flip for line mode
  - Resolution up to 12M@30fps
- Channel3 output:
  - Scale: Bilinear filter (output width no more than 1920)
  - ASPT_RATIO: Aspect Ratio for image boundary extension
  - Output scan order: Line YUV422/YUV420 SP 8bits
  - Flip: Vertical Flip
  - Resolution up to 1920x1080@30fps
- Channel4 output:
  - Scale: Bilinear filter (output width no more than 1920)
  - ASPT_RATIO: Aspect Ratio for image boundary extension
  - Output scan order: Line YUV422/YUV420 SP 8bits
  - Flip: Vertical Flip
  - Resolution up to 1920x1080@30fps
- Channel5 output:
  - Scale: Bilinear filter (output width no more than 1920)
  - ASPT_RATIO: Aspect Ratio for image boundary extension
  - Output scan order: Line YUV422/YUV420 SP 8bits
  - Flip: Vertical Flip
  - Resolution up to 1920x1080@30fps
- Tile4x4 or RKFBCE64x4 of channel0 and channel1 are mutually exclusive

- VPSS_Lite(VPSL)
  - Online or offline input in Luma Pyramid path
  - Online input in Sigma Pyramid path
  - Raw or Y image input format
  - Luma Pyramid multi-band output: Raw mode has 3 channels, Y mode has 6 channels
  - Sigma Pyramid multi-band output: Raw mode has 4 channels, Y mode has 5 channels
  - Maximum image resolution: 4096x3072 (width no more than 4096)
  - Minimum image resolution: 64x64

1.2.12 Serial Audio Interface(SAI)

- Support 3 SAI interfaces
  - SAI 0 support 4 TX lanes and 4 RX lanes
  - SAI 1 support 1 TX lane and 1 RX lane
  - SAI 2 support 1 TX lane and 3 RX lanes
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable
  - Support slot valid data length 8 to 32 bits configurable

- PDM
  - Support up to 8 channels
  - Support resolution is from 16bits to 24bits
  - Support sample rate is up to 192KHz
  - Support PDM master receive mode
  - Support gain control

- ASRC
  - Support dual 2-channel ASRC

- Support sample rate and resample rate range from 8 to 384KHz
- Support real-time transmission mode
- Support memory fetch mode

1.2.13 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus widths

- MAC 10/100/1000M Ethernet
  - Support one Ethernet controllers
  - Support Integrated IEEE 802.3/802.3u compliant 10/100Mbps Ethernet PHY
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support both full-duplex and half-duplex operation
  - Support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO) network acceleration

- USB 2.0 Host
  - Support one USB2.0 Host
  - Compatible with USB 2.0 specification
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- USB 2.0 OTG
  - Compatible Specification
    - Universal Serial Bus Specification, Revision 2.0
    - Extensible Host Controller Interface for Universal Serial Bus (xHCI), Revision1.1
  - Support Control/Bulk/Interrupt/Isochronous Transfer

- SPI interface
  - Support 2 SPI Controllers
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- I2C Master controller
  - Support 6 I2C ports in Master mode
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400K bits/s in the Fast-mode and up to 1M bit/s in high speed mode

- UART interface
  - Support 8 UART ports
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART1~UART7
  - Support RS485 function for UART1~UART7

- PWM
  - Support 4 PWM interface(PWM0-PWM3), total 28 channels
  - Support input capture mode
  - Support continuous mode and one-shot output mode
  - Support two-stage frequency division of working clock
  - PWM0,PWM2~3 support 8 channel (CH0~CH7) with interrupt-based operation

- PWM0,PWM2~3 support biphasic counter
- Only PWM2 support generates waveform through lookup table
- PWM1 support 4 channel (CH0~CH3) with interrupt-based operation
- PWM1 support power key capture mode
- PWM1 support clock frequency meter
- PWM1 support clock counter

- CAN interface
  - 2 CAN ports
  - Compliance to CAN and CAN FD specification
  - Support CAN standard and extended frame
  - Support data frame, remote frame, overload frame, error frame and frame interval
  - Support Internal Storage Mode
  - Support protocol exception event

1.2.14 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support 2 channel TS-ADC (used for CPU and NPU respectively)
  - -40~125°C temperature range and +/-3.5°C temperature accuracy
  - Resolution: 0.01°C

- Successive approximation ADC (SARADC)
  - Support 6 single-ended input channels
  - 13-bit resolution
  - Up to 2MS/s sampling rate
  - Support single mode and series conversion mode

- OTP
  - Support 8K bits size, 6.5K bits for secure application
  - Support Program/Read/Idle mode

- Package Type
  - FCCSP 409-pin (body: 14mm x 14mm; ball size: 0.3mm; ball pitch: 0.65mm)

1.3 Block Diagram

The following figure shows the basic block diagram.

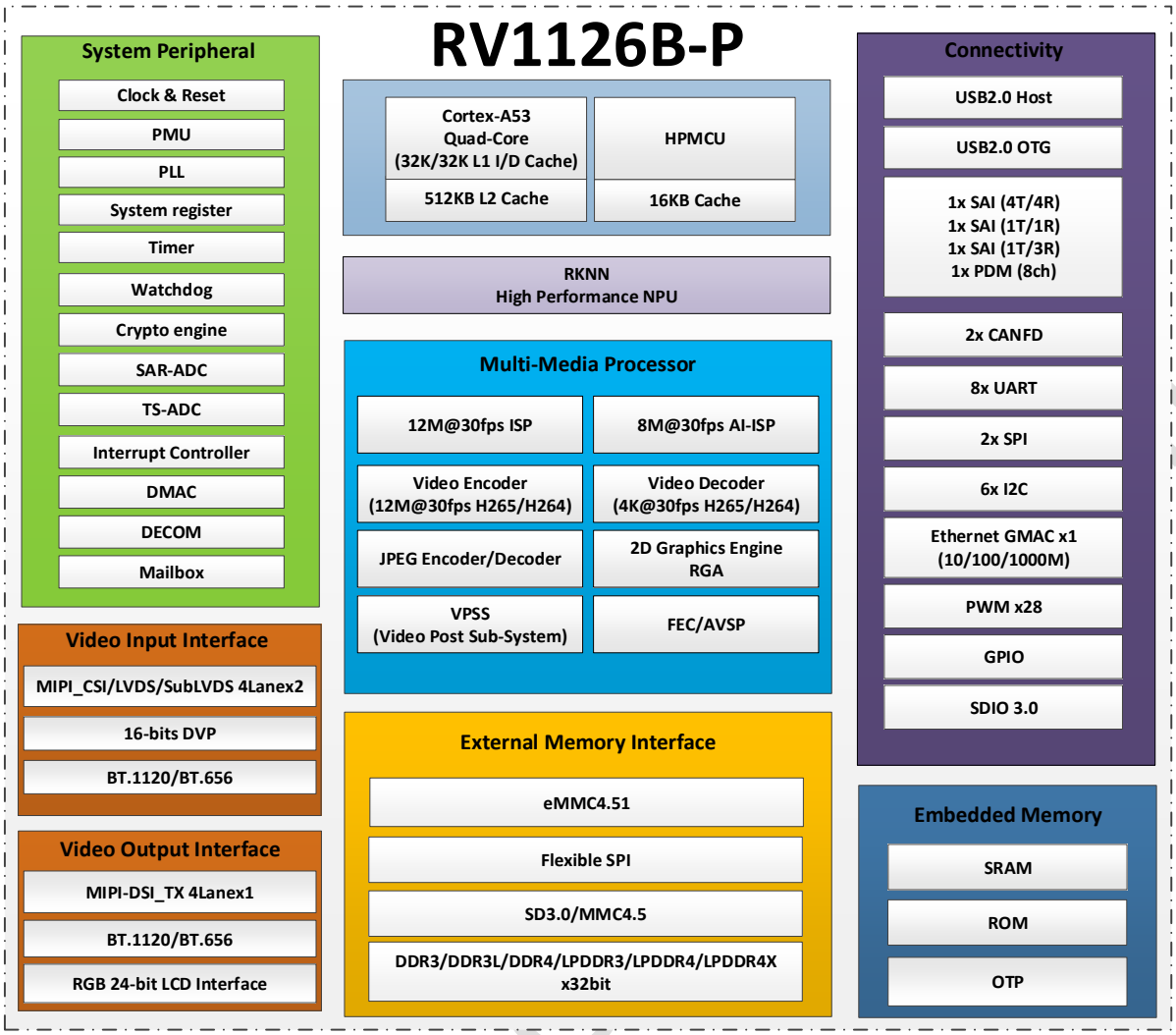


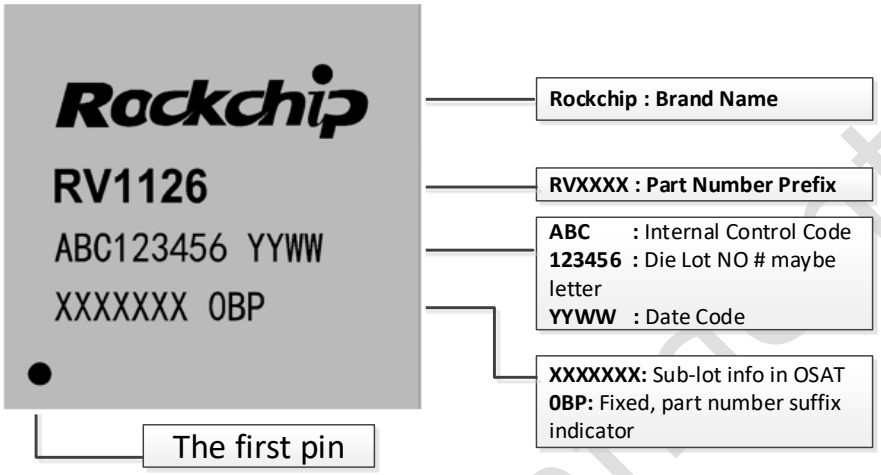
Fig. 1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty	Device Feature
RV1126B-P	RoHS	FCCSP409L	1190pcs	Quad-core application processor

2.2 Top Marking



2.3 Package Dimension

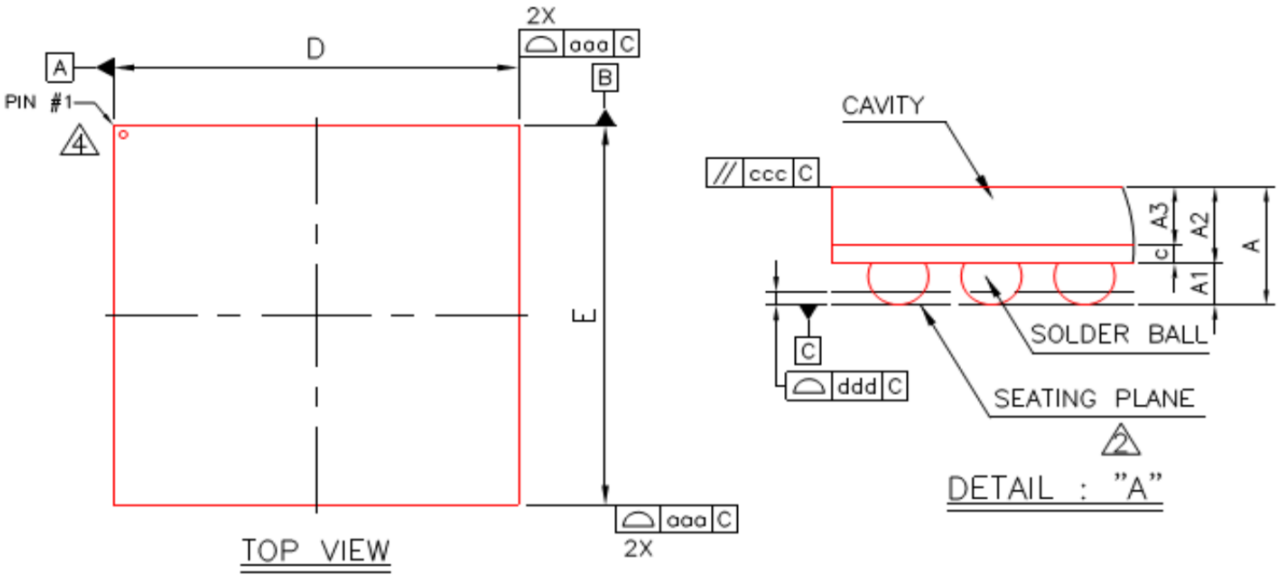


Fig. 2-1 RV1126B-P Package Top and Side View

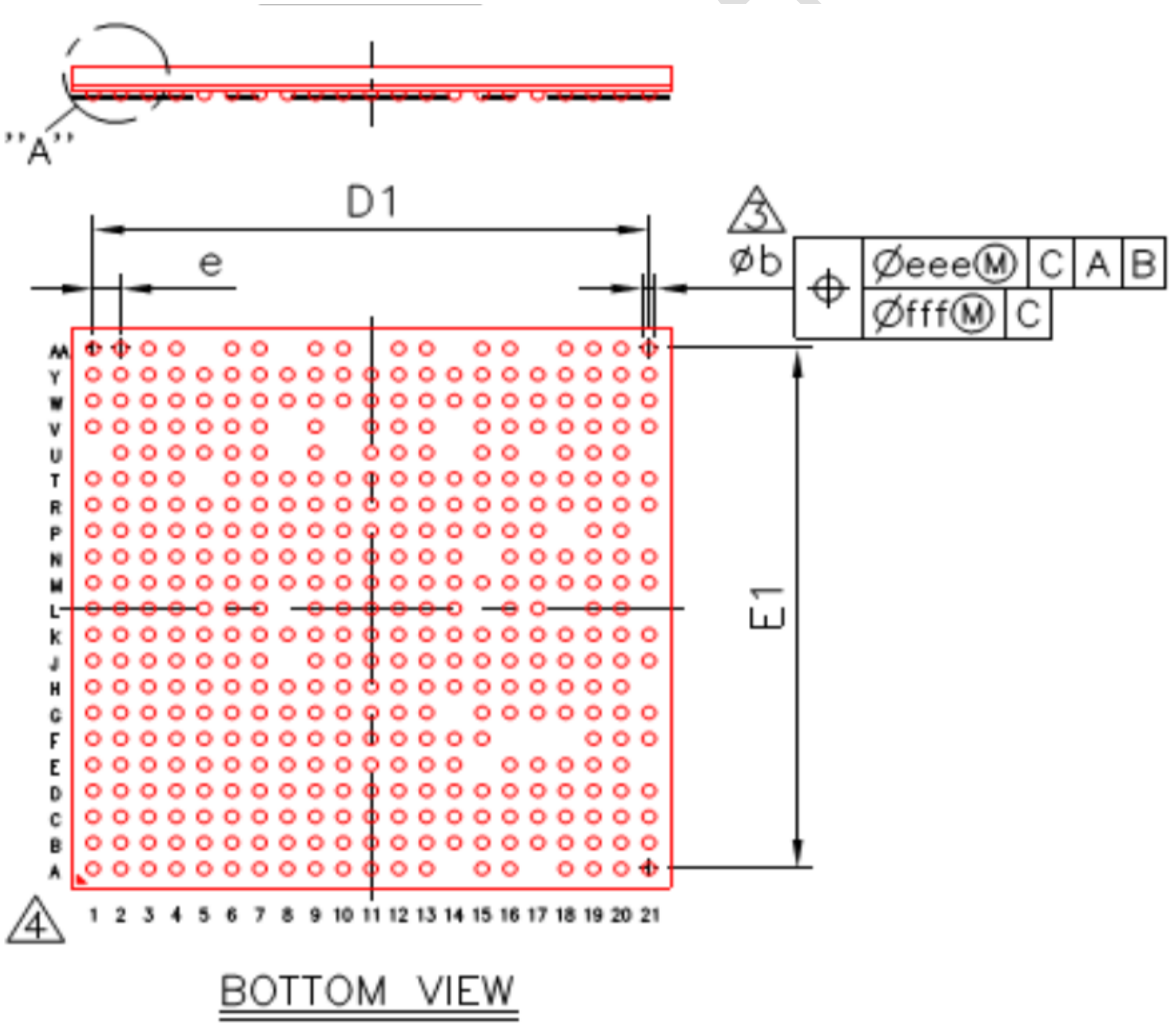


Fig. 2-2 RV1126B-P Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.760	0.830	0.900	0.030	0.033	0.035
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.570	0.620	0.670	0.022	0.024	0.026
A3	0.42	0.45	0.48	0.017	0.018	0.019
c	0.140	0.170	0.200	0.006	0.007	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D1	---	13.00	---	---	0.512	---
E1	---	13.00	---	---	0.512	---
e	---	0.65	---	---	0.026	---
b	0.26	0.31	0.36	0.010	0.012	0.014
aaa	0.15			0.006		
ccc	0.20			0.008		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	21/21					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .
5. BALL PLACEMENT USE 0.30 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING= 0.275 mm.

Fig. 2-3 RV1126B-P Package Dimension

2.4 MSL Information

Moisture sensitivity Level ： MSL3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material ： SnAgCu

2.6 Pin Number List

Table 2-1 RV1126B-P Pin Number Order Information

Pin name	Pin#	Pin name	Pin#
VSS_1	A1	VSS_59	L6
DDR3_DQ24/DDR4_DQU0_B/LPDDR3_DQ30/LPDDR4_DQ8_B	A2	DDR_VDD_7	L7
DDR3_DQ25/DDR4_DQU1_B/LPDDR3_DQ31/LPDDR4_DQ9_B	A3	NC_2	L9
DDR3_CKE/DDR4_ACTN/LPDDR3_CKE/LPDDR4_A3_B	A4	LOGIC_DVDD_2	L10
DDR3_CSN0/DDR4_ODT0/LPDDR3_CSN0/LPDDR4_A4_B	A5	VSS_60	L11
DDR3_WEN/DDR4_BA1/LPDDR4_CKE1_B	A6	VSS_61	L12
DDR3_A12/DDR4_A5/LPDDR4_ODT0_B	A7	VSS_62	L13
DDR3_A1/DDR4_A8/LPDDR3_A1/LPDDR4_CKE0_A	A8	VSS_63	L14
DDR3_A6/DDR4_A4/LPDDR3_A6/LPDDR4_CLKP_A	A9	VSS_64	L16
DDR3_A8/DDR4_A10/LPDDR3_A8/LPDDR4_CLKN_A	A10	VO_LCDC_D1/I2C5_SCL_M2/VI_CIF_D1_M1/SAI2_SDI2_M1/PWM2_CH5_M0/UART4_CTSN_M1/GPIO5_A1	L17
DDR3_A14/DDR4_A14_WEN/LPDDR4_CSN1_B	A11	VO_LCDC_D4/SPI0_MOSI_M2/SAI2_SDO_M1/PWM0_CH3_M1/UART5_TX_M1/GPIO5_A4	L19

Pin name	Pin#	Pin name	Pin#
DDR3_A13/DDR4_A13/LPDDR4_A3_A	A12	VO_LCDC_D5/SPI0_MISO_M2/SAI2_SCLK_M1/PWM0_CH2_M1/UART5_RX_M1/GPIO5_A5	L20
SAI2_SDI1_M0/UART1_RX_M1/I2C5_SDA_M1/GPIO3_B7	A13	DDR3_DQ22/DDR4_DQL6_B/LPDDR3_DQ17/LPDDR4_DQ6_A	M1
UART2_CTSN_M0/GPIO3_A7	A15	DDR3_DM2/DDR4_DML_B/LPDDR3_DM2/LPDDR4_DM0_A	M2
SDMMC1_CMD/GPIO3_A1	A16	VSS_65	M3
SARADC_IN3	A18	DDR3_DQ6/DDR4_DQL6_A/LPDDR3_DQ5/LPDDR4_DQ14_A	M4
MIPI_DPHY_DSI_TX_D0P	A19	VSS_66	M5
MIPI_DPHY_DSI_TX_D1P	A20	DDR_VREFOUT	M6
AVSS_2	A21	VSS_67	M7
DDR3_DQ30/DDR4_DQU6_B/LPDDR3_DQ26/LPDDR4_DQ14_B	B1	VSS_68	M8
DDR3_DQ31/DDR4_DQU7_B/LPDDR3_DQ27/LPDDR4_DQ15_B	B2	NC_3	M9
DDR3_DM3/DDR4_DMU_B/LPDDR3_DM3/LPDDR4_DM1_B	B3	VSS_69	M10
DDR3_ODT0/DDR4_CSN0/LPDDR3_ODT0/LPDDR4_A2_B	B4	LOGIC_DVDD_3	M11
DDR3_A10/DDR4_A15_CASN/LPDDR4_A0_B	B5	VSS_70	M12
DDR3_A15/DDR4_A3/LPDDR4_A5_B	B6	VSS_71	M13
DDR3_BA1/DDR4_A1/LPDDR4_CKE0_B	B7	VSS_72	M14
DDR3_A4/DDR4_A7/LPDDR3_A4/LPDDR4_ODT0_A	B8	VCCIO6_VCC	M15
DDR3_A5/DDR4_A9/LPDDR3_A5/LPDDR4_A5_A	B9	VSS_73	M16
DDR3_A11/DDR4_A16_RASN/LPDDR4_CSN0_B	B10	VI_CIF_D13_M0/ETH_RXCTL_M0/PDM_SDI0_M1/UART7_RX_M1/GPIO6_B5	M17
DDR3_A9/DDR4_A2/LPDDR3_A9/LPDDR4_A4_A	B11	VI_CIF_D14_M0/PDM_SDI1_M1/UART7_RTSN_M1/GPIO6_B6	M18
VSS_3	B12	VI_CIF_CLKIN_M0/ETH_CLK_25M_OUT_M0/PWM0_CH1_M2/UART3_CTSN_M2/GPIO6_C1	M19
SPI1_CSN1_M1/SAI2_MCLK_M0/SDMMC1_DETN/UART1_TX_M1/I2C5_SCL_M1/GPIO3_B6	B13	VO_LCDC_D3/SPI0_CSN0_M2/SAI2_MCLK_M1/PWM0_CH4_M2/UART4_RX_M1/GPIO5_A3	M20
SPI1_MOSI_M1/SAI2_SDO_M0/PWM2_CH0_M0/GPIO3_B2	B14	VO_LCDC_D2/VI_CIF_D2_M1/SAI2_SDI1_M1/PWM0_CH5_M2/UART4_TX_M1/GPIO5_A2	M21
UART2_RTSN_M0/GPIO3_A6	B15	DDR3_DQS2N/DDR4_DQSL_N_B/LPDDR3_DQS2N/LPDDR4_DQS0N_A	N1
SDMMC1_D0/I2C1_SCL_M1/GPIO3_A2	B16	DDR3_DQS2P/DDR4_DQSL_P_B/LPDDR3_DQS2P/LPDDR4_DQS0P_A	N2
SARADC_IN5	B17	DDR3_DM0/DDR4_DML_A/LPDDR3_DM0/LPDDR4_DM1_A	N3
SARADC_IN2	B18	DDR3_DQ3/DDR4_DQL3_A/LPDDR3_DQ0/LPDDR4_DQ11_A	N4
MIPI_DPHY_DSI_TX_D0N	B19	VSS_74	N5
MIPI_DPHY_DSI_TX_D1N	B20	VSS_75	N6
MIPI_DPHY_DSI_TX_D2P	B21	VSS_76	N7

Pin name	Pin#	Pin name	Pin#
DDR3_DQ14/DDR4_DQU6_A/LPDDR3_DQ14/LPDDR4_DQ6_B	C1	NC_4	N8
DDR3_DQ15/DDR4_DQU7_A/LPDDR3_DQ15/LPDDR4_DQ7_B	C2	NC_5	N9
VSS_4	C3	VSS_77	N10
DDR3_RESETN/DDR4_RESETN/LPDDR4_RESETN	C4	VSS_78	N11
VSS_5	C5	CPU_DVDD_0	N12
DDR3_CASN/DDR4_CKE/LPDDR4_A1_B	C6	VSS_79	N13
VSS_6	C7	VSS_80	N14
DDR3_BA2/DDR4_A6/LPDDR4_A0_A	C8	VSS_81	N16
DDR3_A3/DDR4_A0/LPDDR3_A3/LPDDR4_CKE1_A	C9	VI_CIF_D6_M0/ETH_TXD3_M0/PWM2_CH2_M2/UART4_RTSN_M2/GPIO6_A6	N17
VSS_7	C10	VI_CIF_D9_M0/ETH_TXCTL_M0/SPI1_CSN0_M0/SAI0_SDI1_M1/SAI0_SDO3_M1/UART6_RX_M1/GPIO6_B1	N18
DDR3_A7/DDR4_A11/LPDDR3_A7/LPDDR4_A2_A	C11	VI_CIF_D12_M0/ETH_MCLK_M0/SPI1_CLK_M0/PDM_CLK0_M1/UART7_TX_M1/GPIO6_B4	N19
VSS_8	C12	VI_CIF_D15_M0/ETH_MDIO_M0/PDM_CLK1_M1/UART7_CTSN_M1/GPIO6_B7	N20
SPI1_CSN0_M1/SAI2_LRCK_M0/PWM2_CH3_M0/UART1_CTSN_M1/I2C4_SDA_M0/GPIO3_B5	C13	VI_CIF_VSYNC_M0/ETH_MDC_M0/PWM0_CH0_M2/UART3_RTSN_M2/I2C2_SCL_M2/GPIO6_C0	N21
SAI2_SDI2_M0/UART2_TX_M0/GPIO3_B1	C14	DDR3_DQ23/DDR4_DQL7_B/LPDDR3_DQ20/LPDDR4_DQ7_A	P1
SDMMC1_D3/GPIO3_A5	C15	DDR3_DQ20/DDR4_DQL4_B/LPDDR3_DQ21/LPDDR4_DQ4_A	P2
SDMMC1_D1/I2C1_SDA_M1/GPIO3_A3	C16	DDR3_DQ7/DDR4_DQL7_A/LPDDR3_DQ1/LPDDR4_DQ15_A	P3
SARADC_IN4	C17	DDR3_DQ2/DDR4_DQL2_A/LPDDR3_DQ4/LPDDR4_DQ10_A	P4
MIPI_DPHY_DSI_TX_CLKN	C18	VSS_82	P5
MIPI_DPHY_DSI_TX_CLKP	C19	VCCIO1_VCC	P6
MIPI_DPHY_DSI_TX_D2N	C20	VSS_83	P7
VO_LCDC_VSYNC/SPI1_MOSI_M2/PWM1_CH1_M1/UART3_RTSN_M1/GPIO5_D2	C21	VSS_84	P8
DDR3_DQ9/DDR4_DQU1_A/LPDDR3_DQ11/LPDDR4_DQ1_B	D1	VSS_85	P9
DDR3_DQ8/DDR4_DQU0_A/LPDDR3_DQ10/LPDDR4_DQ0_B	D2	PMUIO_VDD_0V9	P10
DDR3_DQS3P/DDR4_DQSU_P_B/LPDDR3_DQS3P/LPDDR4_DQS1P_B	D3	PLL_AVDD_0V9	P11
DDR3_CLKP/DDR4_CLKP/LPDDR3_CLKP/LPDDR4_CLKP_B	D4	CPU_DVDD_1	P12
DDR3_CLKN/DDR4_CLKN/LPDDR3_CLKN/LPDDR4_CLKN_B	D5	CPU_DVDD_2	P13
DDR3_ODT1/DDR4_BG0/LPDDR3_ODT1/LPDDR4_CSN1_A	D6	VSS_86	P14
DDR3_RASN/DDR4_A12/LPDDR4_A1_A	D7	VCCIO4_VCC	P15
DDR3_BA0/DDR4_CSN1	D8	VSS_87	P16

Pin name	Pin#	Pin name	Pin#
VSS_9	D9	VI_CIF_D2_M0/CAN1_RXD_M1/SAI0_SDO0_M1/PWM1_CH2_M2/UART5_TX_M2/I2C4_SCL_M1/GPIO6_A2	P17
DDR3_A0/DDR4_ODT1/LPDDR3_A0/LPDDR4_ODT1_B	D10	VI_CIF_CLKOUT_M0/ETH_TXCLK_M0/PWM0_CH2_M2/UART3_TX_M2/GPIO6_C2	P19
DDR3_A2/DDR4_BG1/LPDDR3_A2/LPDDR4_ODT1_A	D11	VI_CIF_HSYNC_M0/ETH_RXCLK_M0/PWM0_CH3_M2/UART3_RX_M2/I2C2_SDA_M2/GPIO6_C3	P20
VSS_10	D12	VSS_88	R1
SPI1_CLK_M1/SAI2_SCLK_M0/PWM2_CH2_M0/UART1_RTSN_M1/I2C4_SCL_M0/GPIO3_B4	D13	FSPI0_D1/SAI1_SCLK_M0/GPIO1_B5	R2
UART2_RX_M0/GPIO3_B0	D14	FSPI0_CLK/GPIO1_B7	R3
SDMMC1_D2/GPIO3_A4	D15	FSPI0_D3/SAI1_SDI_M0/GPIO1_B6	R4
SDMMC1_CLK/GPIO3_A0	D16	VSS_89	R5
SARADC_IN1	D17	USB_AVDD_0V9	R6
AVSS_11	D18	USB_AVDD_1V8	R7
MIPI_DPHY_DSI_TX_D3N	D19	PMUIO1_VCC	R8
MIPI_DPHY_DSI_TX_D3P	D20	PMUIO0_VCC3V3	R9
VO_LCDC_CLK/SPI1_MISO_M2/PWM1_CH0_M1/UART3_CTSN_M1/GPIO5_D3	D21	NC_6	R10
DDR3_DQ13/DDR4_DQU5_A/LPDDR3_DQ13/LPDDR4_DQ5_B	E1	PLL_AVDD_1V8	R11
DDR3_DM1/DDR4_DMU_A/LPDDR3_DM1/LPDDR4_DM0_B	E2	VSS_90	R12
DDR3_DQS3N/DDR4_DQSU_N_B/LPDDR3_DQS3N/LPDDR4_DQS1N_B	E3	VSS_91	R13
VSS_12	E4	VSS_92	R14
DDR_RZQ	E5	MIPI_DPHY_CSI_RX1_AVDD_0V9	R15
VSS_13	E6	MIPI_DPHY_CSI_RX1_AVDD_1V8	R16
DDR3_CSN1/DDR4_BA0/LPDDR3_CSN1/LPDDR4_CSN0_A	E7	VI_CIF_D0_M0/CAN0_RXD_M1/SAI0_SCLK_M1/PWM1_CH0_M2/UART4_TX_M2/I2C3_SCL_M3/GPIO6_A0	R17
VSS_14	E8	VI_CIF_D3_M0/ETH_RXD2_M0/CAN1_TXD_M1/SAI0_SDI0_M1/PWM1_CH3_M2/UART5_RX_M2/I2C4_SDA_M1/GPIO6_A3	R18
VSS_15	E9	VI_CIF_D7_M0/ETH_TXD0_M0/PWM2_CH3_M2/SAI0_SDI3_M1/SAI0_SDO1_M1/UART4_CTSN_M2/GPIO6_A7	R19
VSS_16	E10	VI_CIF_D10_M0/ETH_RXD0_M0/SPI1_MOSI_M0/PDM_SDI2_M1/UART6_RTSN_M1/GPIO6_B2	R20
VSS_17	E11	VI_CIF_D11_M0/ETH_RXD1_M0/SPI1_MISO_M0/PDM_SDI3_M1/UART6_CTSN_M1/GPIO6_B3	R21
VSS_18	E12	EMMC_CLK/GPIO1_B3	T1
SPI1_MISO_M1/SAI2_SDI0_M0/PWM2_CH1_M0/GPIO3_B3	E13	FSPI0_D0/SAI1_LRCK_M0/GPIO1_B4	T2
VCCIO3_VCC	E14	FSPI0_D2/SAI1_SDO_M0/GPIO1_B2	T3
SARADC_AVDD_1V8	E16	EMMC_CMD/GPIO1_B1	T4

Pin name	Pin#	Pin name	Pin#
SARADC_IN0	E17	VSS_93	T6
MIPI_DSI_TX0_AVDD_0V9	E18	USB_AVDD_3V3	T7
CAN0_TXD_M0/I2C2_SDA_M1/PWM1_CH3_M1/UART3_RX_M1/GPIO5_D5	E19	TVSS	T8
SPI1_CSN1_M2/CAN0_RXD_M0/I2C2_SCL_M1/PWM0_CH7_M2/UART3_TX_M1/GPIO5_D4	E20	VSS_94	T9
DDR3_DQS1N/DDR4_DQSU_N_A/LPDDR3_DQS1N/LPDDR4_DQS0N_B	F1	VSS_95	T10
DDR3_DQS1P/DDR4_DQSU_P_A/LPDDR3_DQS1P/LPDDR4_DQS0P_B	F2	SAI0_SDI3_M0/SAI0_SDO1_M0/PDM_SDI3_M0/UART2_RTSN_M1/GPIO7_A7	T11
VSS_19	F3	VCCIO7_VCC	T12
DDR3_DQ27/DDR4_DQU3_B/LPDDR3_DQ29/LPDDR4_DQ11_B	F4	VCCIO2_VCC	T13
VSS_20	F5	VSS_96	T14
DDR_AVSS	F6	MIPI_DPHY_CSI_RX0_AVDD_0V9	T15
VSS_21	F7	MIPI_DPHY_CSI_RX0_AVDD_1V8	T16
VSS_22	F8	VSS_97	T17
VSS_23	F9	VI_CIF_D1_M0/CAN0_TXD_M1/SAI0_LRCK_M1/PWM1_CH1_M2/UART4_RX_M2/I2C3_SDA_M3/GPIO6_A1	T18
VSS_24	F10	VI_CIF_D4_M0/ETH_RXD3_M0/SAI0_MCLK_M1/PWM2_CH0_M2/UART5_RTSN_M2/I2C5_SCL_M3/GPIO6_A4	T19
VSS_25	F11	VI_CIF_D5_M0/ETH_TXD2_M0/PWM2_CH1_M2/UART5_CTSN_M2/I2C5_SDA_M3/GPIO6_A5	T20
VSS_26	F12	VI_CIF_D8_M0/ETH_TXD1_M0/SPI1_CSN1_M0/SAI0_SDI2_M1/SAI0_SDO2_M1/UART6_TX_M1/GPIO6_B0	T21
VSS_27	F13	FSPI0_CSN0/SAI1_MCLK_M0/GPIO1_B0	U2
AVSS_28	F14	EMMC_D7/GPIO1_A7	U3
AVSS_29	F15	EMMC_D6/GPIO1_A6	U4
VO_LCDC_D23/ETH_RXCLK_M1/VI_CIF_HSYNC_M1/SAI1_SDI_M2/PWM3_CH7_M1/GPIO5_C7	F19	NC_7	U5
VO_LCDC_D22/ETH_TXCLK_M1/VI_CIF_CLKIN_M1/SAI1_LRCK_M2/PWM3_CH6_M1/GPIO5_C6	F20	NC_8	U6
VO_LCDC_D21/ETH_TXD2_M1/VI_CIF_CLKOUT_M1/SAI1_SCLK_M2/PWM3_CH5_M1/GPIO5_C5	F21	SDMMC0_DETN/PWM1_CH0_M0/GPIO0_A5	U7
DDR3_DQ12/DDR4_DQU4_A/LPDDR3_DQ12/LPDDR4_DQ4_B	G1	PWM0_CH2_M0/UART1_RTSN_M0/GPIO0_C6	U9
VSS_30	G2	SAI0_SDI2_M0/SAI0_SDO2_M0/PDM_SDI2_M0/DSM_AUD_RN/I2C1_SCL_M3/UART2_RX_M1/GPIO7_B0	U11
DDR3_DQ29/DDR4_DQU5_B/LPDDR3_DQ25/LPDDR4_DQ13_B	G3	SAI0_MCLK_M0/PWM2_CH6_M1/GPIO7_A2	U12
DDR3_DQ26/DDR4_DQU2_B/LPDDR3_DQ28/LPDDR4_DQ10_B	G4	SDMMC0_D3/UART3_TX_M0/UART4_CTSN_M3/JTAG_TMS_M1/GPIO2_A3	U13
VSS_31	G5	MIPI_DPHY_CSI_RX0_CLKP	U15
VSS_32	G6	MIPI_DPHY_CSI_RX0_D0N	U16

Pin name	Pin#	Pin name	Pin#
DDR_VDD_1	G7	SPI0_MISO_M1/SAI1_LRCK_M1/I2C3_SDA_M1/GPIO4_A5	U18
DDR_VDD_2	G8	SPI0_CSN0_M1/SAI1_SDI_M1/UART5_TX_M0/I2C4_SDA_M2/GPIO4_A6	U19
DDR_VDD_3	G9	SPI0_CLK_M1/SAI1_SDO_M1/UART5_RX_M0/I2C4_SCL_M2/GPIO4_A7	U20
VSS_33	G10	EMMC_D5/FSPI0_CSN1/GPIO1_A5	V1
VSS_34	G11	EMMC_D4/GPIO1_A4	V2
VSS_35	G12	EMMC_D3/GPIO1_A3	V3
VSS_36	G13	EMMC_D2/GPIO1_A2	V4
MIPI_DSI_TX0_AVDD_1V8	G15	USB_OTG_VBUSDET	V5
AVSS_37	G16	SPI0_MOSI_M0/GPIO0_B0	V6
AVSS_38	G17	SPI0_CSN1_M0/GPIO0_A6	V7
UART0_TX_M1/JTAG_TCK_M2/CAN1_RXD_M0/PWM2_CH6_M0/GPIO5_D6	G18	PWM0_CH1_M0/UART1_RX_M0/I2C5_SDA_M0/GPIO0_C5	V9
VO_LCDC_D19/ETH_RXD2_M1/VI_CIF_D15_M1/SAI1_MCLK_M2/PWM3_CH3_M1/GPIO5_C3	G19	SAI0_SDI1_M0/SAI0_SDO3_M0/PDM_SDI1_M0/DSM_AUD_RP/I2C1_SDA_M3/UART2_TX_M1/GPIO7_B1	V11
VO_LCDC_D18/ETH_TXCTL_M1/VI_CIF_D14_M1/PWM3_CH2_M1/GPIO5_C2	G20	I2C4_SCL_M3/PDM_CLK1_M0/PWM2_CH5_M1/GPIO7_A1	V12
VO_LCDC_D17/ETH_CLK_25M_OUT_M1/VI_CIF_D13_M1/PWM3_CH1_M1/GPIO5_C1	G21	SDMMC0_D2/UART3_RX_M0/UART4_RTSN_M3/JTAG_TCK_M1/GPIO2_A2	V13
DDR3_DQ11/DDR4_DQU3_A/LPDDR3_DQ9/LPDDR4_DQ3_B	H1	MIPI_DPHY_CSI_RX0_CLKN	V15
DDR3_DQ10/DDR4_DQU2_A/LPDDR3_DQ8/LPDDR4_DQ2_B	H2	MIPI_DPHY_CSI_RX0_D0P	V16
DDR3_DQ28/DDR4_DQU4_B/LPDDR3_DQ24/LPDDR4_DQ12_B	H3	VSS_98	V17
VSS_39	H4	MIPI_DPHY_CSI_RX1_CLKP	V18
VSS_40	H5	SPI0_MOSI_M1/SAI1_SCLK_M1/I2C3_SCL_M1/GPIO4_A4	V19
VSS_41	H6	SPI0_CSN1_M1/SAI1_MCLK_M1/UART4_TX_M0/GPIO4_A3	V20
VSS_42	H7	CAM_CLK0_OUT/UART5_CTSN_M0/GPIO4_B1	V21
DDR_VDD_4	H8	EMMC_D1/GPIO1_A1	W1
LOGIC_DVDD_0	H9	EMMC_D0/GPIO1_A0	W2
VSS_43	H10	USB_OTG_DP	W3
NPU_DVDD_0	H11	USB_OTG_DM	W4
NPU_DVDD_1	H12	SPI0_MISO_M0/GPIO0_B1	W5
LOGIC_DVDD_4	H13	REF_CLK0_OUT/TEST_CLK0_OUT/GPIO0_A0	W6
OTP_VCC_1V8	H14	NPOR_DET	W7
VSS_44	H15	PWM0_CH0_M0/UART1_TX_M0/I2C5_SCL_M0/GPIO0_C4	W8
UART0_RX_M1/JTAG_TMS_M2/CAN1_TXD_M0/PWM2_CH7_M0/GPIO5_D7	H16	VSS_99	W9
VO_LCDC_HSYNC/SPI1_CLK_M2/I2C3_SDA_M2/PWM1_CH2_M1/GPIO5_D1	H17	I2C3_SCL_M0/PWM0_CH7_M0/GPIO0_C0	W10

Pin name	Pin#	Pin name	Pin#
VO_LCDC_D20/ETH_RXD3_M1/VI_CIF_VSYNC_M1/SAI1_SDO_M2/PWM3_CH4_M1/GPIO5_C4	H18	SAI0_LRCK_M0/DSM_AUD_LN/PWM2_CH7_M1/GPIO7_A3	W11
VO_LCDC_D16/ETH_TXD1_M1/VI_CIF_D12_M1/PWM3_CH0_M1/GPIO5_C0	H19	SAI0_SCLK_M0/PWM2_CH4_M1/GPIO7_A0	W12
VO_LCDC_D15/ETH_TXD0_M1/VI_CIF_D11_M1/PWM2_CH3_M1/UART7_CTSN_M0/GPIO5_B7	H20	SDMMC0_D1/UART0_TX_M0/I2C0_SCL_M1/GPIO2_A1	W13
DDR3_DQ18/DDR4_DQL2_B/LPDDR3_DQ23/LPDDR4_DQ2_A	J1	VSS_100	W14
DDR3_DQ19/DDR4_DQL3_B/LPDDR3_DQ22/LPDDR4_DQ3_A	J2	MIPI_DPHY_CSI_RX0_D2P	W15
DDR3_DQ4/DDR4_DQL4_A/LPDDR3_DQ3/LPDDR4_DQ12_A	J3	MIPI_DPHY_CSI_RX0_D1N	W16
DDR3_DQ1/DDR4_DQL1_A/LPDDR3_DQ6/LPDDR4_DQ9_A	J4	MIPI_DPHY_CSI_RX1_D3N	W17
VSS_45	J5	MIPI_DPHY_CSI_RX1_CLKN	W18
VSS_46	J6	UART4_RTSN_M0/I2C1_SDA_M2/GPIO4_A0	W19
DDR_VDD_5	J7	UART4_RX_M0/GPIO4_A2	W20
LOGIC_DVDD_1	J9	CAM_CLK1_OUT/UART5_RTSN_M0/GPIO4_B0	W21
NPU_DVDD_2	J10	USB_HOST_DP	Y1
NPU_DVDD_3	J11	USB_HOST_DM	Y2
VSS_47	J12	USB_OTG_ID	Y3
LOGIC_DVDD_5	J13	SPI0_CLK_M0/GPIO0_B2	Y4
VSS_48	J14	PWM1_CH1_M0/TSADC_SHUT/TSADC_SHUTORG/GPIO0_A1	Y5
VCCIO5_VCC_0	J15	I2C2_SDA_M0/PWM0_CH5_M0/GPIO0_D1	Y6
VSS_49	J16	I2C0_SDA_M0/GPIO0_C3	Y7
VO_LCDC_DEN/SPI1_CSN0_M2/I2C3_SCL_M2/PWM0_CH6_M2/GPIO5_D0	J17	NC_9	Y8
VO_LCDC_D0/ETH_TXD3_M1/VI_CIF_D0_M1/PWM2_CH4_M0/UART4_RTSN_M1/GPIO5_A0	J18	OSC_XOUT	Y9
VO_LCDC_D12/VI_CIF_D8_M1/UART7_TX_M0/GPIO5_B4	J19	I2C3_SDA_M0/PWM0_CH6_M0/PWR_CRTL2/GPIO0_C1	Y10
VO_LCDC_D14/ETH_MDC_M1/VI_CIF_D10_M1/PWM2_CH2_M1/UART7_RTSN_M0/GPIO5_B6	J20	SAI0_SDO0_M0/DSM_AUD_LP/GPIO7_A5	Y11
VO_LCDC_D13/ETH_MDIO_M1/VI_CIF_D9_M1/UART7_RX_M0/GPIO5_B5	J21	I2C4_SDA_M3/PDM_CLK0_M0/UART2_CTSN_M1/GPIO7_A4	Y12
DDR3_DQ16/DDR4_DQL0_B/LPDDR3_DQ19/LPDDR4_DQ0_A	K1	SDMMC0_CMD/UART3_CTSN_M0/UART4_TX_M3/GPIO2_A5	Y13
DDR3_DQ17/DDR4_DQL1_B/LPDDR3_DQ18/LPDDR4_DQ1_A	K2	SDMMC0_D0/UART0_RX_M0/I2C0_SDA_M1/GPIO2_A0	Y14
DDR3_DQ5/DDR4_DQL5_A/LPDDR3_DQ7/LPDDR4_DQ13_A	K3	MIPI_DPHY_CSI_RX0_D2N	Y15
DDR3_DQ0/DDR4_DQL0_A/LPDDR3_DQ2/LPDDR4_DQ8_A	K4	MIPI_DPHY_CSI_RX0_D1P	Y16
VSS_50	K5	MIPI_DPHY_CSI_RX1_D3P	Y17
VSS_51	K6	MIPI_DPHY_CSI_RX1_D2N	Y18

Pin name	Pin#	Pin name	Pin#
DDR_VDD_6	K7	MIPI_DPHY_CSI_RX1_D1N	Y19
VSS_52	K8	MIPI_DPHY_CSI_RX1_D0N	Y20
VSS_53	K9	UART4_CTSN_M0/I2C1_SCL_M2/GPIO4_A1	Y21
NPU_DVDD_4	K10	VSS_101	AA1
NPU_DVDD_5	K11	SPI0_CSN0_M0/GPIO0_A7	AA2
VSS_54	K12	CLK_32K/GPIO0_A2	AA3
VSS_55	K13	PWM0_CH3_M0/UART1_CTSN_M0/GPIO0_C7	AA4
VSS_56	K14	I2C2_SCL_M0/PWM0_CH4_M0/GPIO0_D0	AA6
VCCIO5_VCC_1	K15	I2C0_SCL_M0/GPIO0_C2	AA7
VO_LCDC_D6/SPI0_CLK_M2/SAI2_SDI0_M1/PWM0_CH1_M1/UART5_RTSN_M1/GPIO5_A6	K16	OSC_XIN	AA9
VO_LCDC_D7/SPI0_CSN1_M2/VI_CIF_D3_M1/SAI2_LRCK_M1/I2C5_SDA_M2/PWM0_CH0_M1/UART5_CTSN_M1/GPIO5_A7	K17	VSS_102	AA10
VO_LCDC_D8/ETH_RXCTL_M1/VI_CIF_D4_M1/UART6_TX_M0/GPIO5_B0	K18	SAI0_SDI0_M0/PDM_SDI0_M0/GPIO7_A6	AA12
VO_LCDC_D9/ETH_RXD0_M1/VI_CIF_D5_M1/UART6_RX_M0/GPIO5_B1	K19	SDMMC0_CLK/UART3_RTSN_M0/UART4_RX_M3/GPIO2_A4	AA13
VO_LCDC_D10/ETH_RXD1_M1/VI_CIF_D6_M1/PWM2_CH0_M1/UART6_RTSN_M0/GPIO5_B2	K20	MIPI_DPHY_CSI_RX0_D3P	AA15
VO_LCDC_D11/ETH_MCLK_M1/VI_CIF_D7_M1/PWM2_CH1_M1/UART6_CTSN_M0/GPIO5_B3	K21	MIPI_DPHY_CSI_RX0_D3N	AA16
DDR3_DQ21/DDR4_DQL5_B/LPDDR3_DQ16/LPDDR4_DQ5_A	L1	MIPI_DPHY_CSI_RX1_D2P	AA18
VSS_57	L2	MIPI_DPHY_CSI_RX1_D1P	AA19
DDR3_DQS0N/DDR4_DQSL_N_A/LPDDR3_DQS0N/LPDDR4_DQS1N_A	L3	MMIPI_DPHY_CSI_RX1_D0P	AA20
DDR3_DQS0P/DDR4_DQSL_P_A/LPDDR3_DQS0P/LPDDR4_DQS1P_A	L4	VSS_103	AA21
VSS_58	L5		

2.7 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-2 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_ XIN	I	Clock input of 24M crystal XO
	OSC_ XOUT	O	Clock output of 24M crystal XO
	REF_CLK0_OUT	O	24M Clock out
	CAM_CLK*i*_OUT (*i*=0~1)	O	Reference Clock Output for external Sensor chip
	CLK_32K	I/O	32K clock If configured as input，clock is provided from external circuit；

Interface	Pin Name	Direction	Description
			If configured as output，clock is provided from internal circuit of chip；
	PWR_CTRL*2*	O	Chip low power mode output indication signal

Interface	Pin Name	Direction	Description
SW-DP	JTAG_TCK_M*i* (*i*=0~2)	I	SWD interface clock input
	JTAG_TMS_M*i* (*i*=0~2)	I/O	SWD interface data input/output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	eMMC card clock
	EMMC_CMD	I/O	eMMC card command output and response input
	EMMC_D[*i*] (*i*=0~7)	I/O	eMMC card data input and output

Interface	Pin Name	Direction	Description
SPI	SPI*i*_CLK_M*j* (i=0,1)(*j*=0~2)	I/O	SPI serial clock
	SPI*i*_CSN0_M*j* (i=0,1)(*j*=0~2)	I/O	SPI chip select signal, low active
	SPI*i*_CSN1_M*j* (i=0,1)(*j*=0~2)	O	SPI chip select signal, low active
	SPI*i*_MOSI_M*j* (i=0,1)(*j*=0~2)	I/O	SPI serial data input
	SPI*i*_MISO_M*j* (i=0,1)(*j*=0~2)	I/O	SPI serial data output

Interface	Pin Name	Direction	Description
FSPI0 Controller	FSPI0_CLK	O	FSPI0 serial clock
	FSPI0_CSN0_M*j* (j=0,1)	O	FSPI0 chip select0 signal, low active
	FSPI0_Di(i=0~3)	I/O	FSPI0 serial data input/output signal

Interface	Pin Name	Direction	Description
SD/MMC/ SDIO Host Controller	SDMMCi_CLK	O	SDMMC card clock
	SDMMCi_CMD	I/O	SDMMC card command output and response input
	SDMMCi_D[*j*] (*i*=0~1)(j=0~3)	I/O	SDMMC card data input and output

Interface	Pin Name	Direction	Description
SAI0 Controller	SAI0_MCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM reference clock
	SAI0_SCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI0_LRCK_M*j* (j=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI0_SDO*i*_M*j* (*i*=0~3)(j=0~1)	O	I2S/PCM/TDM serial data output
	SAI0_SDI*i*_M*j* (*i*=0~3)(j=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1 Controller	SAI1_MCLK_M*j* (j=0~2)	I/O	I2S/PCM/TDM reference clock
	SAI1_SCLK_M*j*	I/O	I2S/PCM/TDM serial clock

Interface	Pin Name	Direction	Description
	(j=0~2)		
	SAI1_LRCK_M*j* (j=0~2)	I/O	I2S/PCM/TDM channel indication signal
	SAI1_SDO_M*j* (j=0~2)	O	I2S/PCM/TDM serial data output
	SAI1_SDI_M*j* (j=0~2)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI2 Controller	SAI2_MCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM reference clock
	SAI2_SCLK_M*j* (j=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI2_LRCK_M*j* (j=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI2_SDO_M*j* (j=0~1)	O	I2S/PCM/TDM serial data output
	SAI2_SDI*i*_M*j* (*i*=0~2)(j=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0_CH*i*_Mj(*i*=0~7)(j=0,1,2)	I/O	Pulse Width Modulation input and output
	PWM1_CH*i*_Mj(*i*=0~3) (j=0,1,2)	I/O	Pulse Width Modulation input and output
	PWM2_CH*i*_Mj(*i*=0~7) (j=0,1,2)	I/O	Pulse Width Modulation input and output
	PWM3_CH*i*_Mj(*i*=0~7) (j=0,1)	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C	I2C*0*_SDA_Mj (j=0,1)	I/O	I2C0 data
	I2C*0*_SCL_Mj (j=0,1)	O	I2C0 clock
	I2C*2*_SDA_Mj (j=0,1,2)	I/O	I2C2 data
	I2C*2*_SCL_Mj (j=0,1,2)	O	I2C2 clock
	I2C*i*_SDA_Mj (*i*=1,3,4,5)(j=0~3)	I/O	I2C data
	I2C*i*_SCL_Mj (*i*=1,3,4,5)(j=0~3)	O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX_Mj (*i*=0,3,5) (j=0,1,2)	I	UART serial data input
	UART*i*_TX_Mj (*i*=0,3,5) (j=0,1,2)	O	UART serial data output
	UART*i*_CTSN_Mj (*i*=0,3,5) (j=0,1,2)	I	UART clear to send modem status input
	UART*i*_RTSN_Mj (*i*=0,3,5) (j=0,1,2)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
UART	UART*i*_RX_Mj (*i*=1,2,6,7)	I	UART serial data input

Interface	Pin Name	Direction	Description
	(j=0,1)		
	UART*i*_TX_Mj (*i*=1,2,6,7) (j=0,1)	O	UART serial data output
	UART*i*_CTSN_Mj (*i*=1,2,6,7) (j=0,1)	I	UART clear to send modem status input
	UART*i*_RTSN_Mj (*i*=1,2,6,7) (j=0,1)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
UART	UART*4*_RX_Mj (j=0,1,2,3)	I	UART serial data input
	UART*4*_TX_Mj (j=0,1,2,3)	O	UART serial data output
	UART*4*_CTSN_Mj (j=0,1,2,3)	I	UART clear to send modem status input
	UART*4*_RTSN_Mj (j=0,1,2,3)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
MIPI_RX	MIPI_DPHY_CSI_RX*i*_CK0N (i=0,1)	I	MIPI_RX PHY negative clock input
	MIPI_DPHY_CSI_RX*i*_CK0P (i=0,1)	I	MIPI_RX PHY positive clock input
	MIPI_DPHY_CSI_RX*i*_CK1N (i=0,1)	I	MIPI_RX PHY negative clock input
	MIPI_DPHY_CSI_RX*i*_CK1P (i=0,1)	I	MIPI_RX PHY positive clock input
	MIPI_DPHY_CSI_RX*i*_D*j*N (i=0,1)(j=0~3)	I	MIPI_RX PHY negative data input
	MIPI_DPHY_CSI_RX*i*_D*j*P (i=0,1)(j=0~3)	I	MIPI_RX PHY positive data input

Interface	Pin Name	Direction	Description
MIPI_TX	MIPI_DPHY_DSI_TX_CKN	O	MIPI_TX PHY negative clock output
	MIPI_DPHY_DSI_TX_CKP	O	MIPI_TX PHY positive clock output
	MIPI_DPHY_DSI_TX_D*j*N (j=0~3)	O	MIPI_TX PHY negative data output
	MIPI_DPHY_DSI_TX_D*j*P (j=0~3)	O	MIPI_TX PHY positive data output

Interface	Pin Name	Direction	Description
USB 2.0 Host	USB_HOST_DP	I/O	USB 2.0 Data signal DP
	USB_HOST_DM	I/O	USB 2.0 Data signal DM

Interface	Pin Name	Direction	Description
USB 2.0 OTG	USB_OTG_DP	I/O	USB 2.0 Data signal DP
	USB_OTG_DM	I/O	USB 2.0 Data signal DM

Interface	Pin Name	Direction	Description
	USB_OTG_VBUSDET	I	Insert detect when act as USB device
	USB_OTG_ID	I	USB Mini-Receptacle Identifier

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_ DVDD	0	1.15	V
Supply voltage for NPU	NPU_DVDD	0	1.1	V
Supply voltage for LOGIC	LOGIC_DVDD	0	1.1	V
Supply voltage for PMUIO0	PMUIO0_VCC3V3	0	3.8	V
Supply voltage for PMUIO1	PMUIO1_VCC	0	3.8	V
Supply voltage for VCCIO1	VCCIO1_VCC	0	3.8	V
Supply voltage for VCCIO2	VCCIO2_VCC	0	3.8	V
Supply voltage for VCCIO3	VCCIO3_VCC	0	3.8	V
Supply voltage for VCCIO4	VCCIO4_VCC	0	3.8	V
Supply voltage for VCCIO5	VCCIO5_VCC	0	3.8	V
Supply voltage for VCCIO6	VCCIO6_VCC	0	3.8	V
Supply voltage for VCCIO7	VCCIO7_VCC	0	3.8	V
0.9V supply voltage	PLL_AVDD_0V9 MIPI_DPHY_CSI_RX0_AVDD_0V9 MIPI_DPHY_CSI_RX1_AVDD_0V9 MIPI_DPHY_DSI_TX_AVDD_0V9 USB_AVDD_0V9 PMUIO_VDD0V9	0	1.1	V
1.8V supply voltage	SARADC_AVDD_1V8 PLL_AVDD_1V8 USB_AVDD_1V8 MIPI_DPHY_CSI_RX0_AVDD_1V8 MIPI_DPHY_CSI_RX1_AVDD_1V8 MIPI_DPHY_DSI_TX_AVDD_1V8	0	2.0	V
3.3V supply voltage	USB_AVDD_3V3	0	3.8	V
Supply voltage for DDR IO	DDR_VDDQ	0	1.65	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Related Power Group	Min	Typ	Max	Unit
Supply voltage for CPU	CPU_ DVDD	TBD	0.95	1.1	V
Supply voltage for NPU	NPU_DVDD	TBD	0.95	1.1	V
Supply voltage for LOGIC	LOGIC_DVDD	TBD	0.9	0.99	V
Supply voltage for PMUIO0	PMUIO0_VCC3V3	2.97	3.3	3.63	V
Supply voltage for PMUIO1	PMUIO1_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO1	VCCIO1_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO2	VCCIO2_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO3	VCCIO3_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO4	VCCIO4_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO5	VCCIO5_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V

Parameters	Related Power Group	Min	Typ	Max	Unit
Supply voltage for VCCIO6	VCCIO6_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO7	VCCIO7_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
DDR3 IO VDDQ power	DDR_VDDQ	1.425	1.5	1.575	V
DDR3L IO VDDQ Power	DDR_VDDQ	1.283	1.35	1.417	V
LPDDR3 IO VDDQ Power	DDR_VDDQ	0.994	1.2	1.3	V
DDR4 IO VDDQ Power	DDR_VDDQ	0.994	1.2	1.3	V
LPDDR4 IO VDDQ Power	DDR_VDDQ	1.0	1.1	1.21	V
LPDDR4X IO VDDQ Power	DDR_VDDQL	0.54	0.6	0.66	V
0.9V supply voltage	PLL_AVDD_0V9 MIPI_DPHY_CSI_RX0_AVDD_0V9 MIPI_DPHY_CSI_RX1_AVDD_0V9 MIPI_DPHY_DSI_TX_AVDD_0V9 USB_AVDD_0V9 PMUIO_VDD0V9	0.81	0.9	0.99	V
1.8V supply voltage	SARADC_AVDD_1V8 PLL_AVDD_1V8 USB_AVDD_1V8 MIPI_DPHY_CSI_RX0_AVDD_1V8 MIPI_DPHY_CSI_RX1_AVDD_1V8 MIPI_DPHY_DSI_TX_AVDD_1V8	1.62	1.8	1.98	V
3.3V supply voltage	USB_AVDD3V3	2.97	3.3	3.63	V
Ambient Operating Temperature	Ta	TBD	25	TBD	℃

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

Parameters		Symbol	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @DDR3L mode	Input High Voltage	Vih_ddr	VREF + 0.09	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.09	V
	Output High Voltage	Voh_ddr	VREF + 0.09	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.09	V
DDR IO @DDR4 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V

Parameters		Symbol	Min	Typ	Max	Unit
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @ LPDDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @LPDDR4 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @LPDDR4X mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQL	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQL	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V

Parameters		Symbol	Min	Typ	Max	Unit
MIPI IO@ MIPI HS receiver mode	Common-mod voltage HS receive mode	VCMRX(DC)	70	NA	300	mV
	Differential input high threshold	VIDTH	NA	NA	70	mV
	Differential input low threshold	VIDTL	-70	NA	NA	mV
	Single-ended input high voltage	VIHHS	NA	NA	460	mV
	Single-ended input low voltage	VILHS	-40	NA	NA	mV
	Single-ended threshold for HS termination enable	VTERM-EN	NA	NA	450	mV
	Differential input impedance	ZID	80	100	125	ohm
MIPI IO@ MIPI LP receiver mode	Logic 1 input voltage	VIH	880	NA	NA	mV
	Logic 0 input voltage, not in ULP State	VIL	NA	NA	550	mV
	Logic 0 input voltage, ULP State	VIL-ULPS	NA	NA	300	mV
	Input hysteresis	VHYST	25	NA	NA	mV
MIPI IO@ 1.8V TTL RX mode	Logic 1 input voltage	VIH	1.2	NA	1.58	V
	Logic 0 input voltage, not in ULP State	VIL	NA	NA	0.6	V
	Input hysteresis	VHYST	25	NA	NA	mV

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
			Vin = 1.8V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA

Note: VDDO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Int PLL	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	10	NA	800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	475	NA	1900	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	9	NA	1900	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	1000	1500	Input clock cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Frac PLL	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① *REFDIV is the input divider value;*
② *FBDIV is the feedback divider value;*
③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-7 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for DDR IO

Table 3-8 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current		@ 1.5V , 125℃	-80		6	uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	-65		5	uA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃	-50		4	uA
DDR IO @LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	-50		4	uA
DDR IO @LPDDR4 mode	Input leakage current		@ 1.1V , 125℃	-45		3.5	uA
DDR IO @LPDDR4X mode	Input leakage current		@ 0.6V , 125℃	-20		1.5	uA

3.8 Electrical Characteristics for MIPI DSI

Table 3-9 Electrical Characteristics for MIPI DSI

Parameters	Symbol	Min	Typ	Max	Units
Common-mode variations above 450 MHz	ΔVcmtx(HF)	NA	NA	15	mVrms
Common-mode variations between 50MHz – 450MHz	ΔVcmtx(LF)	NA	NA	25	mVpeak
20%-80% rise time and fall time	Tr and Tf	NA	NA	0.3	UI
		100	NA	NA	ps

3.9 Electrical Characteristics for MIPI CSI interface

Table 3-10 HS Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Typ	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	60	pF

Table 3-11 LP Receiver AC specifications (for MIPI mode)

Parameters	Symbol	Min	Typ	Max	Unit
Input pulse rejection	eSPIKE	NA	NA	300	V.ps
Minimum pulse width response	TMIN-RX	20	NA	NA	ns
Peak interference amplitude	VINT	NA	NA	200	mv
Interference frequency	fINT	450	NA	NA	MHz

Table 3-12 HS Receiver AC specifications (for LVDS mode)

Parameters	Symbol	Min	Typ	Max	Unit
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)	NA	NA	100	mV
Common-mode interference 50MHz – 450MHz	ΔVCMRX(LF)	-50	NA	50	mV
Common-mode termination	CCM	NA	NA	50	pF

3.10 Electrical Characteristics for SARADC

Table 3-13 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution	ENOB	f_S=1MS/s fclk=24MHz	NA	11.2	13	bit

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Analog Input Channel			NA	NA	8	
Analog Input Range	VIN		0	NA	1.8	V
Analog Input maximum voltage					3.3	V
Differential Non-Linearity	DNL		NA	±1	±3	LSB
Integral Non-Linearity	INL		NA	±2	±6	LSB
Conversion Rage	f_S		NA	1	NA	MS/s
Signal to Noise and Distortion Ratio	SINAD	f_S=1MS/s f_{OUT}=1.17KHz	NA	69.2	NA	dB
Total Harmonic Distortion	THD		NA	77.3	NA	dB

3.11 Electrical Characteristics for TSADC

Table 3-14 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±3.5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.01	NA	℃

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	28.5022	(℃/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	4.88	(℃/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	1.4973	(℃/W)	(3)
Thermal characterization parameter	ψ_{JT}	0.1195	(℃/W)	(4)

*Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.（The PCB is 4 layers, 114.5 mm*101.5 mm）*

Note (2): ϑ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance ϑ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψ_{JT} is measured in the test environment of ϑ_{JA} (JEDEC JESD51-2 standard).